Welcome To

ISSCC 2014
Session 21
Frequency Generation Techniques

21.1: A 1.7GHz MDLL-Based Fractional-N Frequency Synthesizer with 1.4ps RMS Integrated Jitter and 3mW Power Using a 1b TDC

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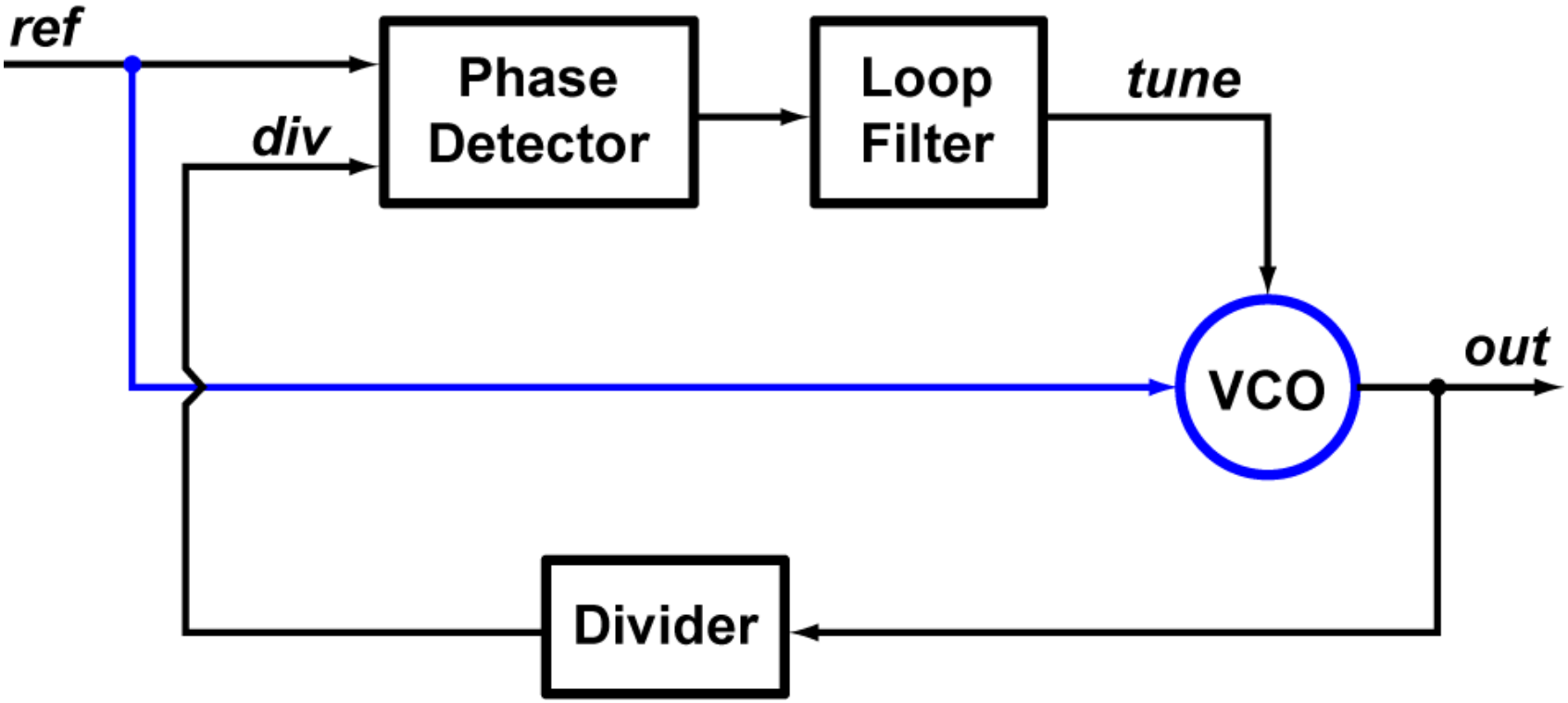
Motivation

- **Fractional-N frequency synthesizers rely on PLL architectures with LC oscillators to achieve good power/jitter performance**
- **Inductor-less implementations scale with process, but compromise efficiency**
- **How can we recover good power/jitter performance in inductor-less fractional-N synthesizers?**

Outline

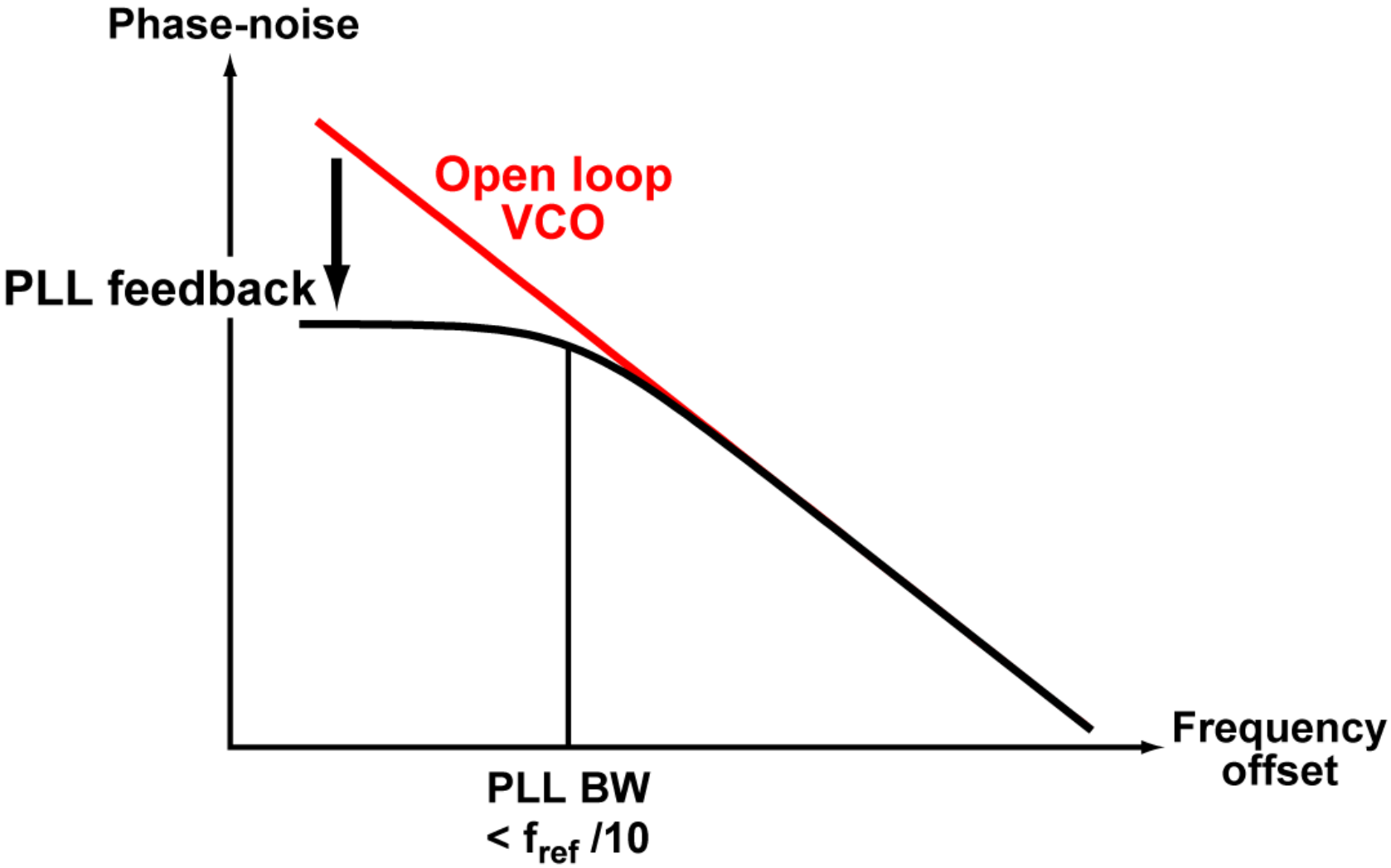
- **State of the art**
- **Proposed architecture**
- **Practical implementation**
- **Measurement results**
- **Conclusion**

State-of-the-art: Inj.-Locked PLL

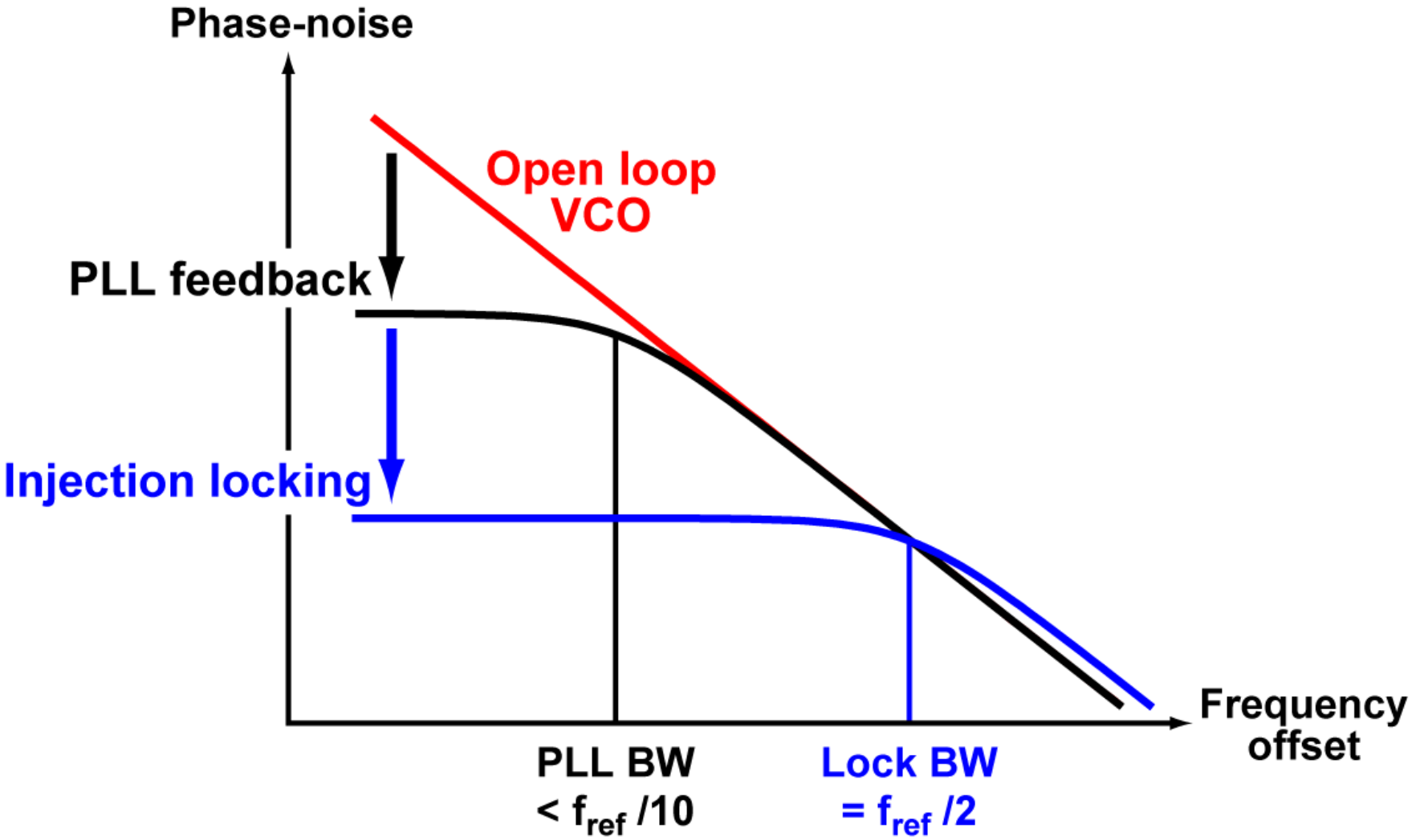


- **Provides additional VCO phase-noise suppression w.r.t. conventional PLL**

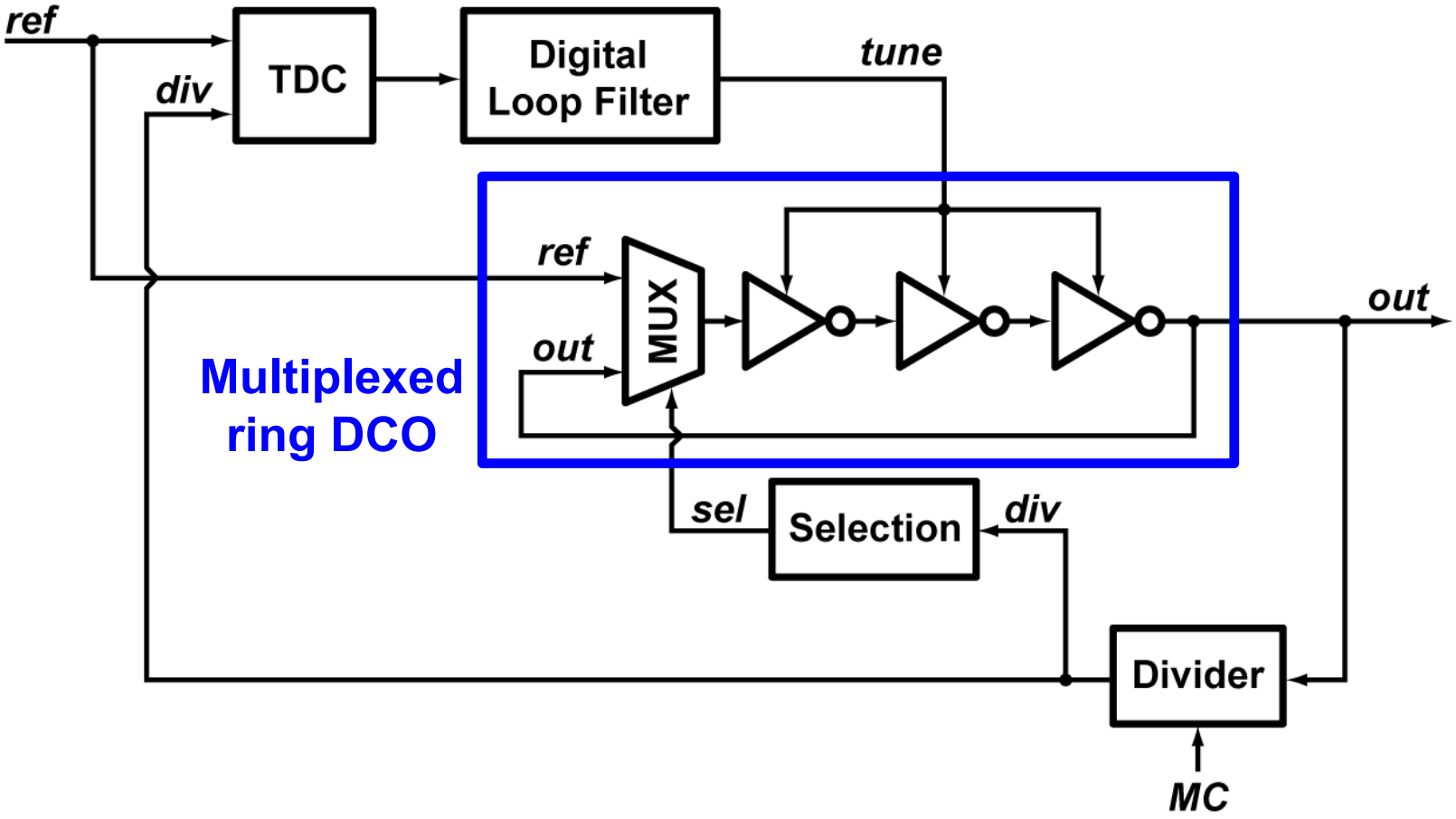
Phase Noise with Injection Locking



Phase Noise with Injection Locking

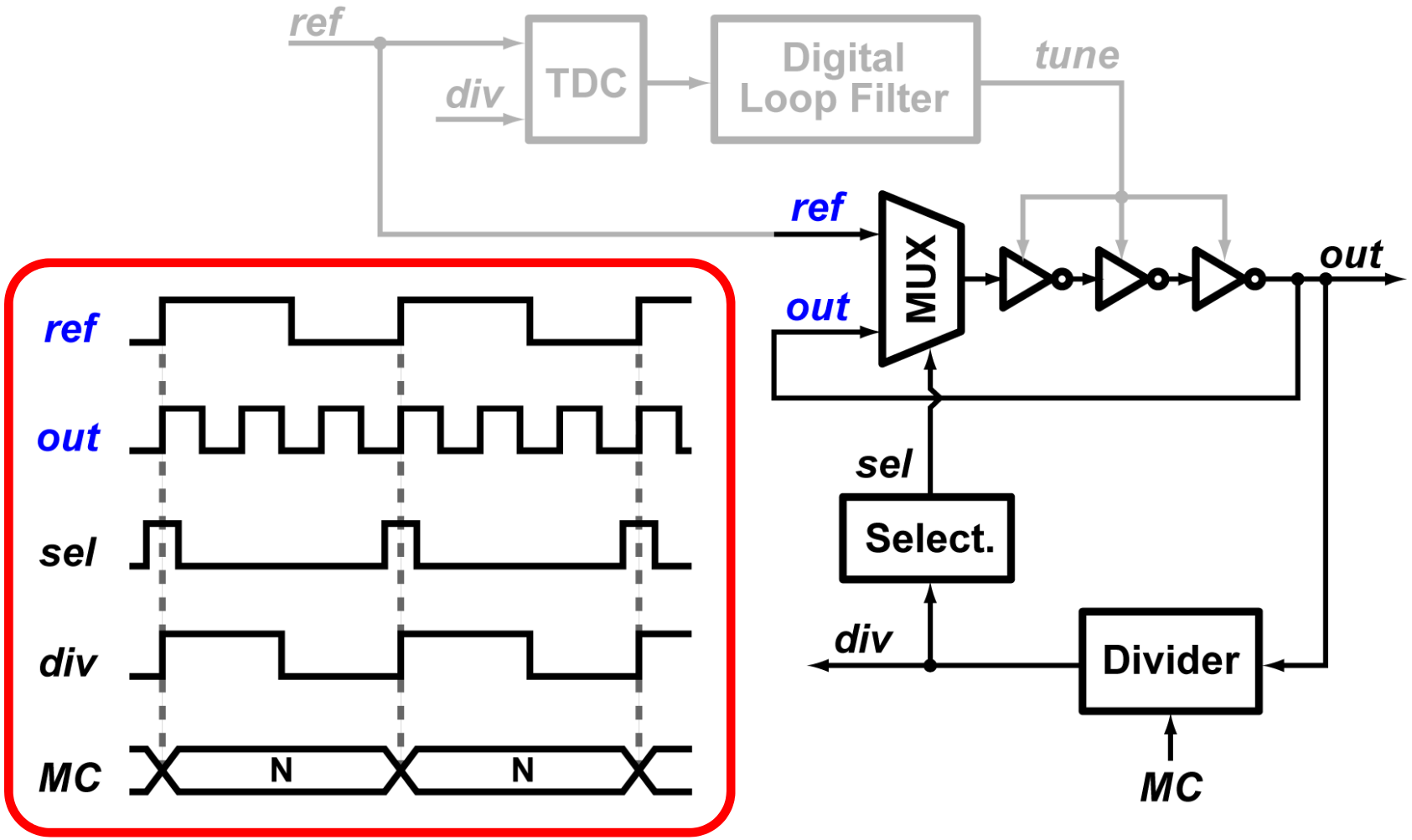


State-of-the-art: MDLL-based PLL



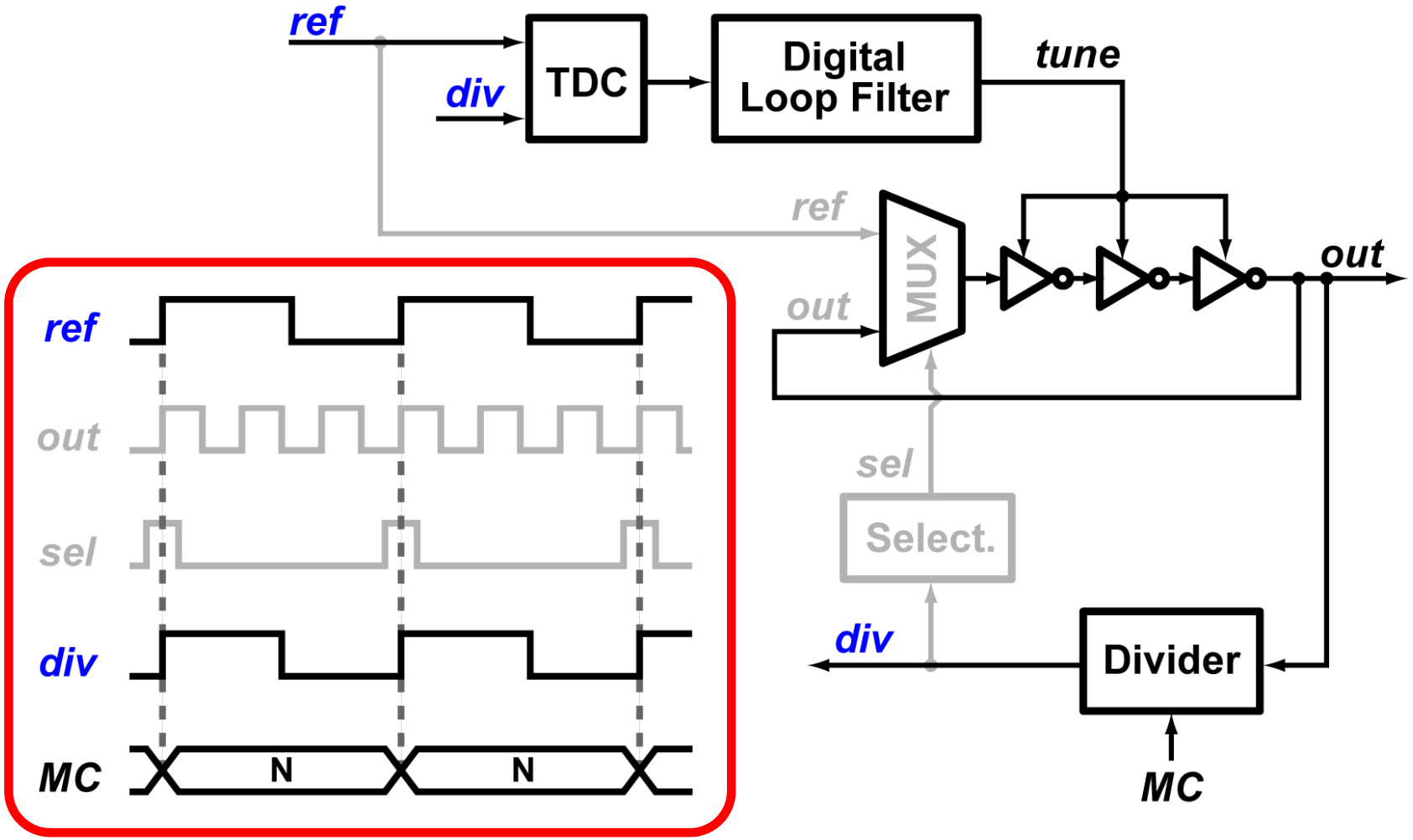
- Multiplying delay-locked loop (MDLL)

MDLL Feedback



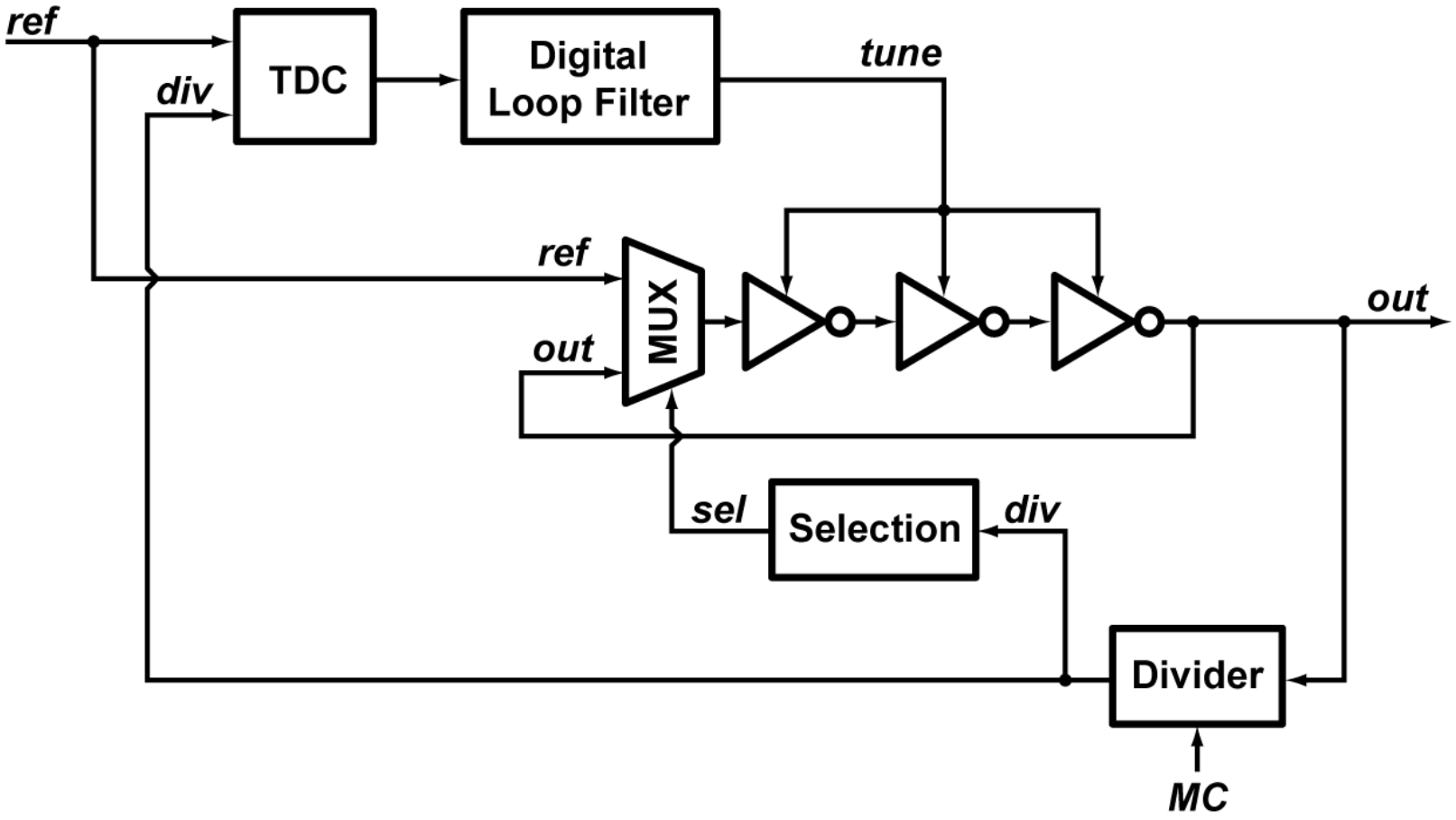
- Every Nth *out* edge is replaced by *ref* edge

PLL Feedback



- No time error is detected by TDC

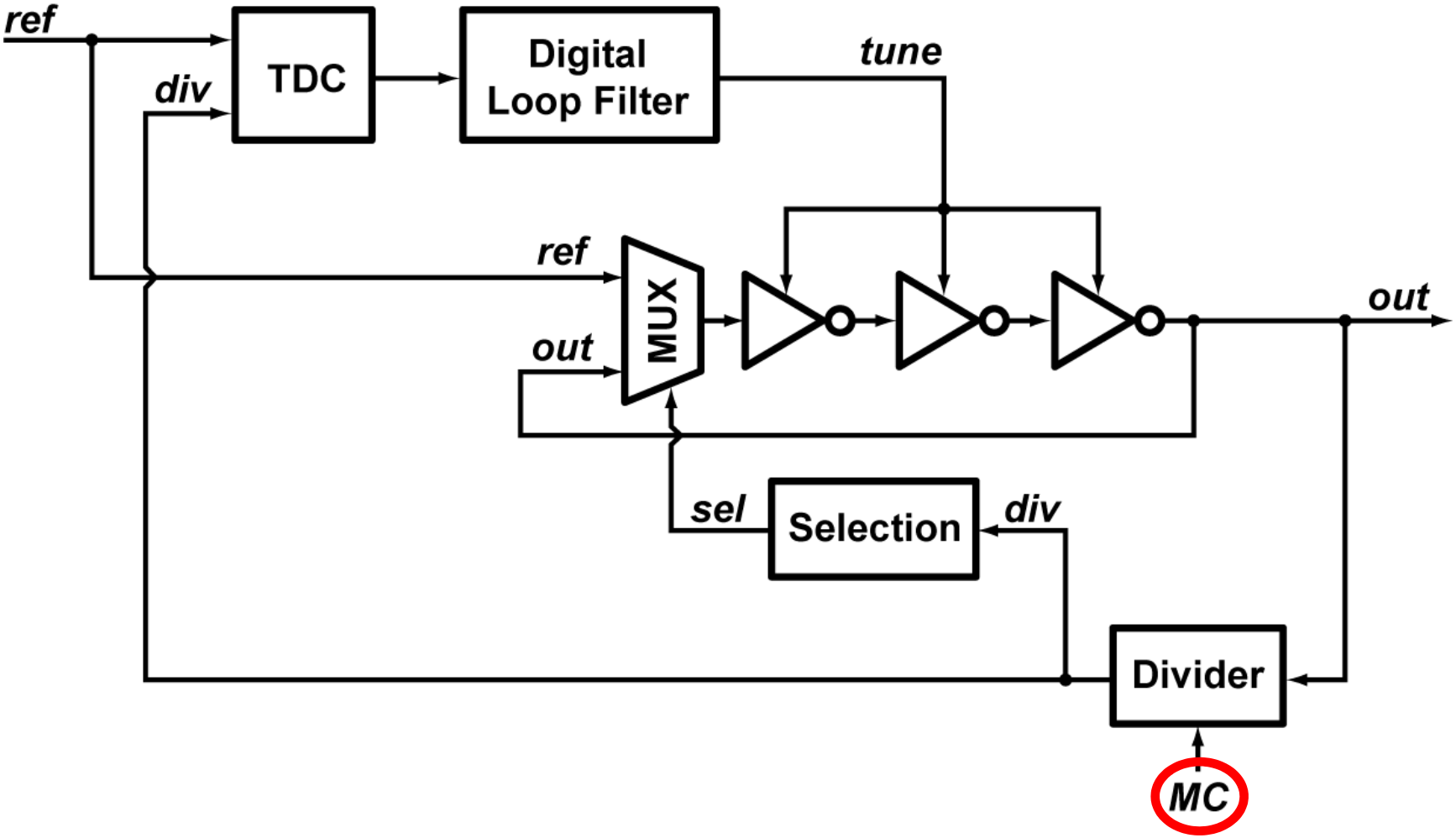
Challenge



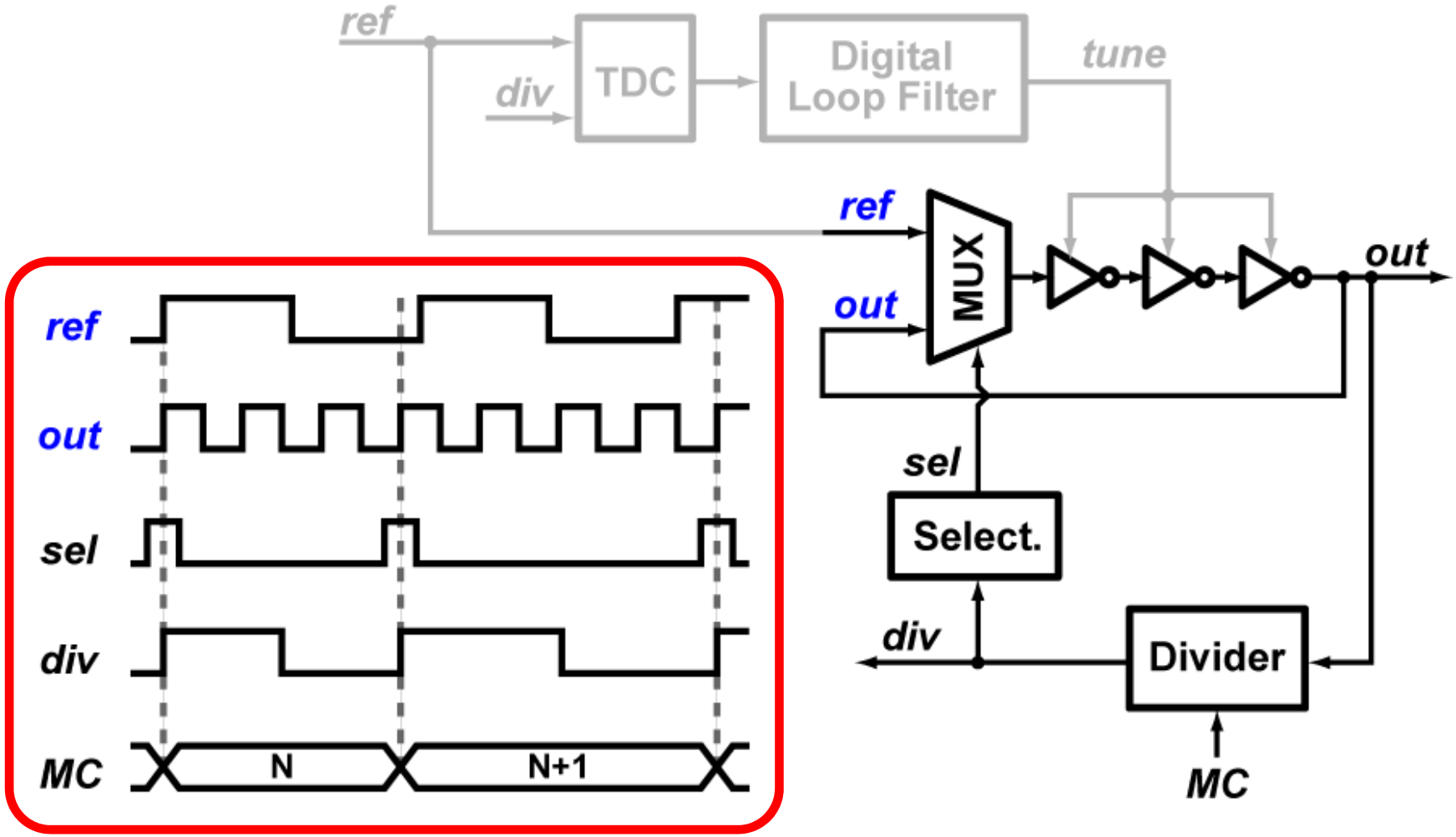
- **Only limited to integer-N channels**

How can we design a fractional-N MDLL-based synthesizer?

Can we simply Dither Divider MC?

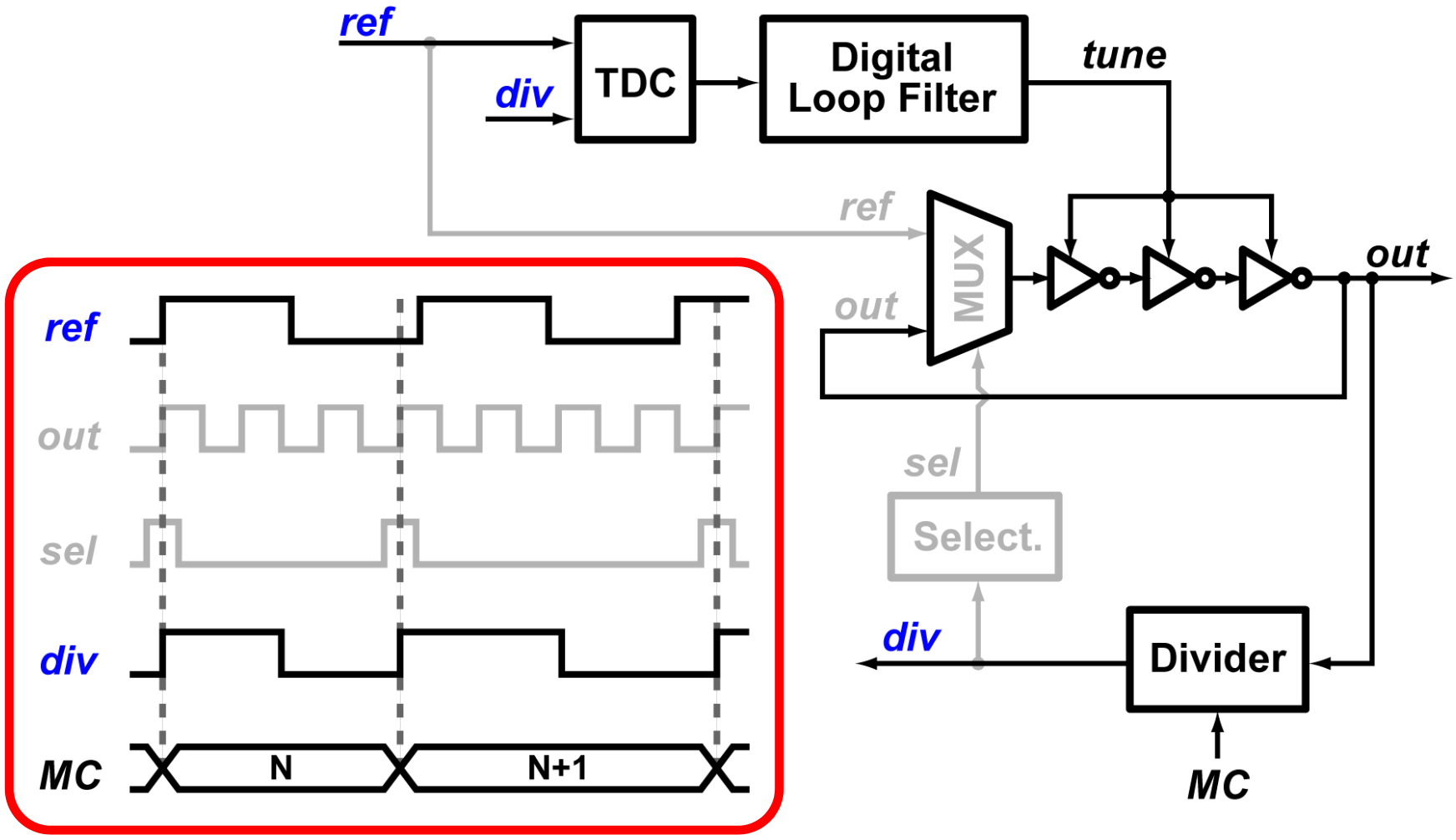


MDLL Feedback after MC Dithering



- *out* edges cannot be replaced by *ref* edges

PLL Feedback after MC Dithering

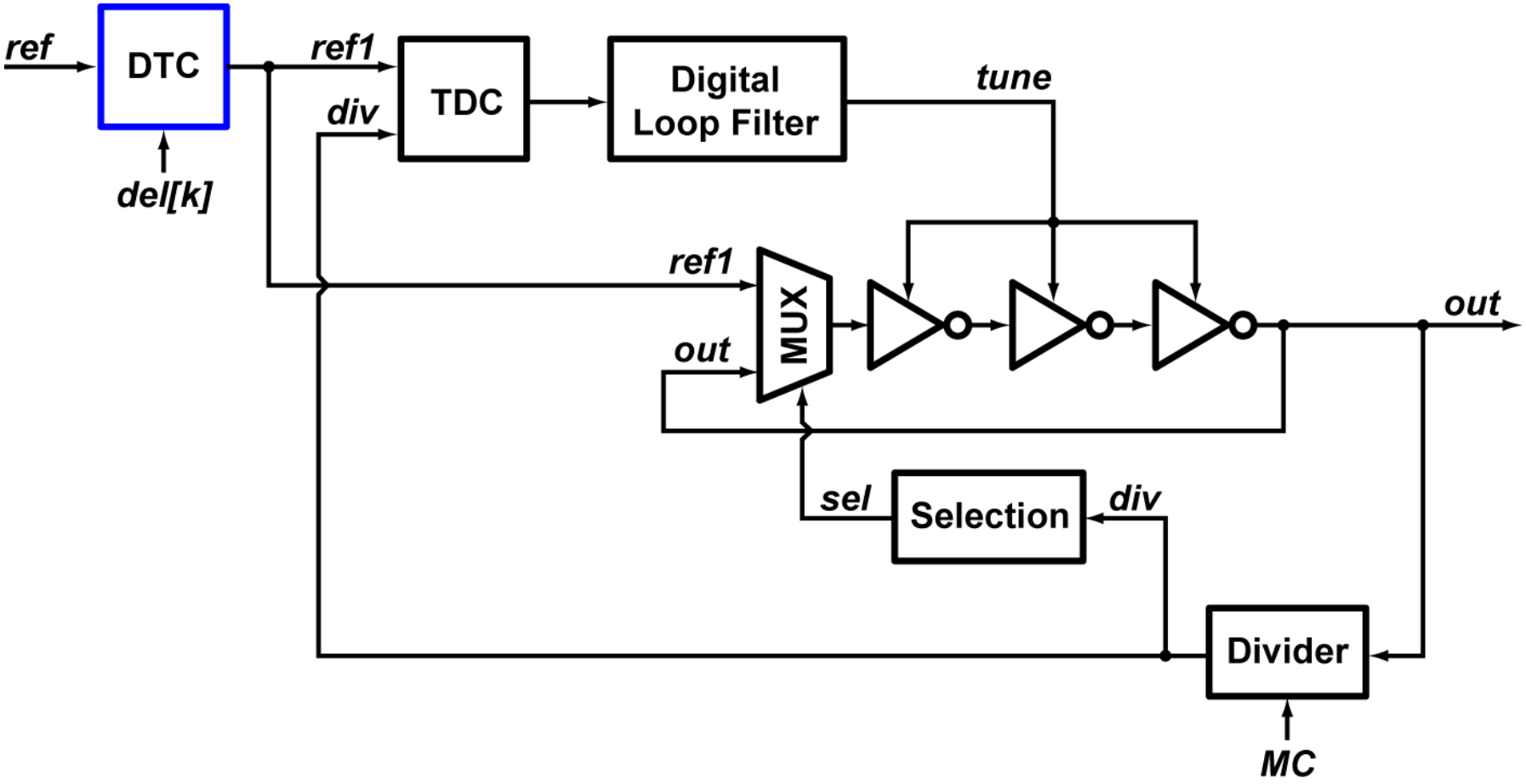


- Very large error at TDC input

Outline

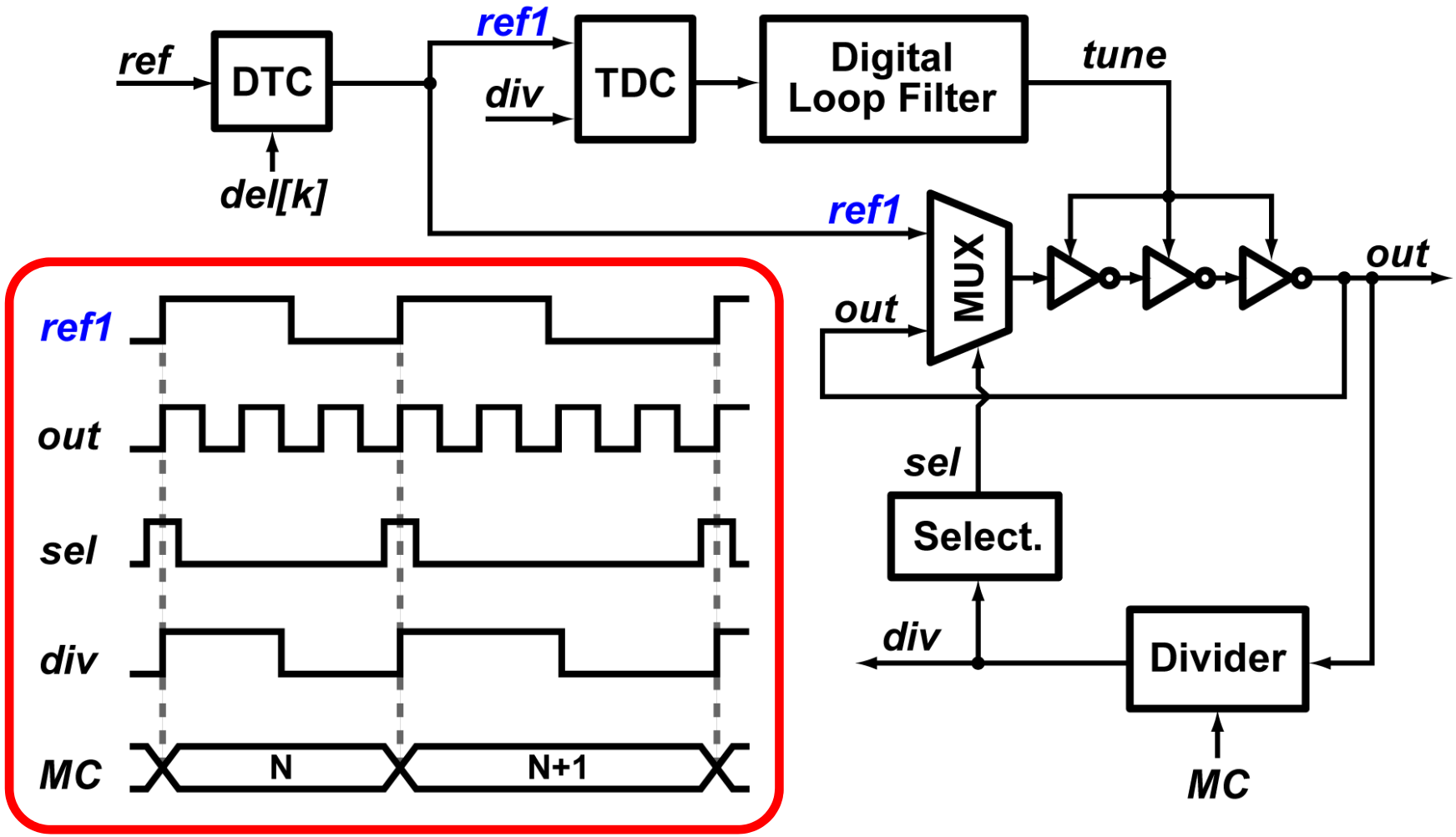
- State of the art
- **Proposed architecture**
- Practical implementation
- Measurement results
- Conclusion

Proposed Fractional-N MDLL



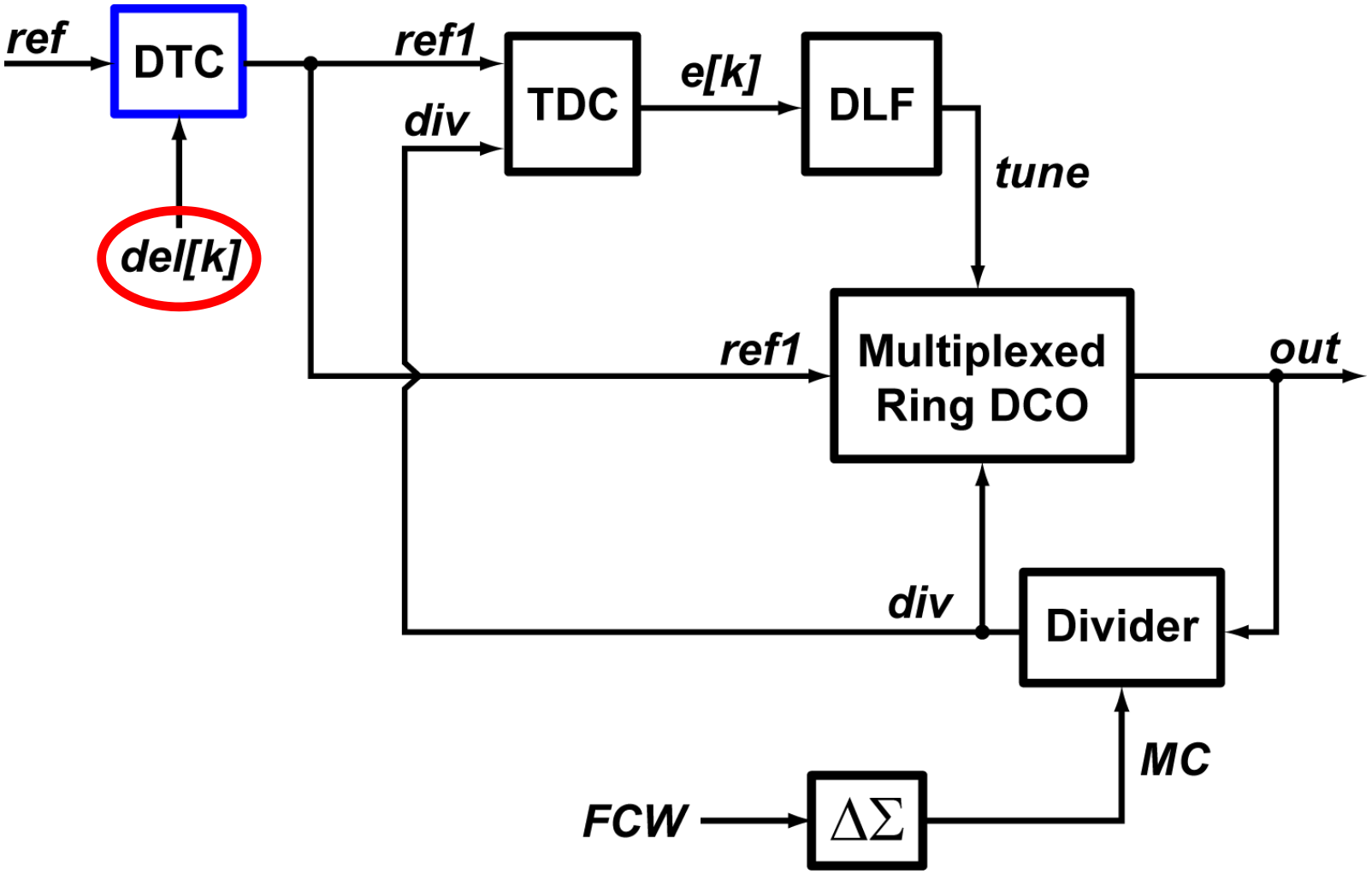
- **We should first realign reference to output via a digital/time converter (DTC)**

Signals after Realignment

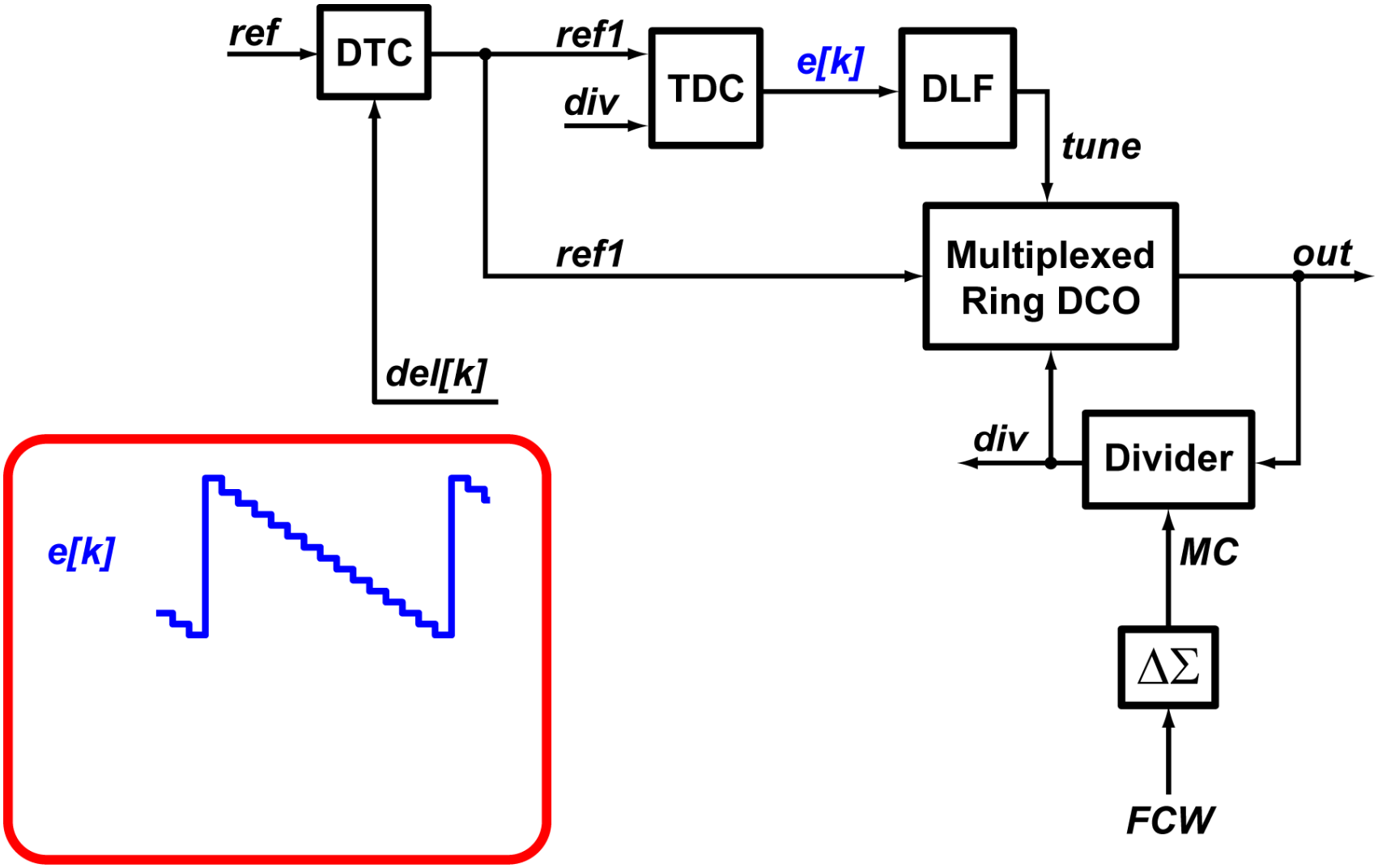


- No time error detected in fractional-N mode

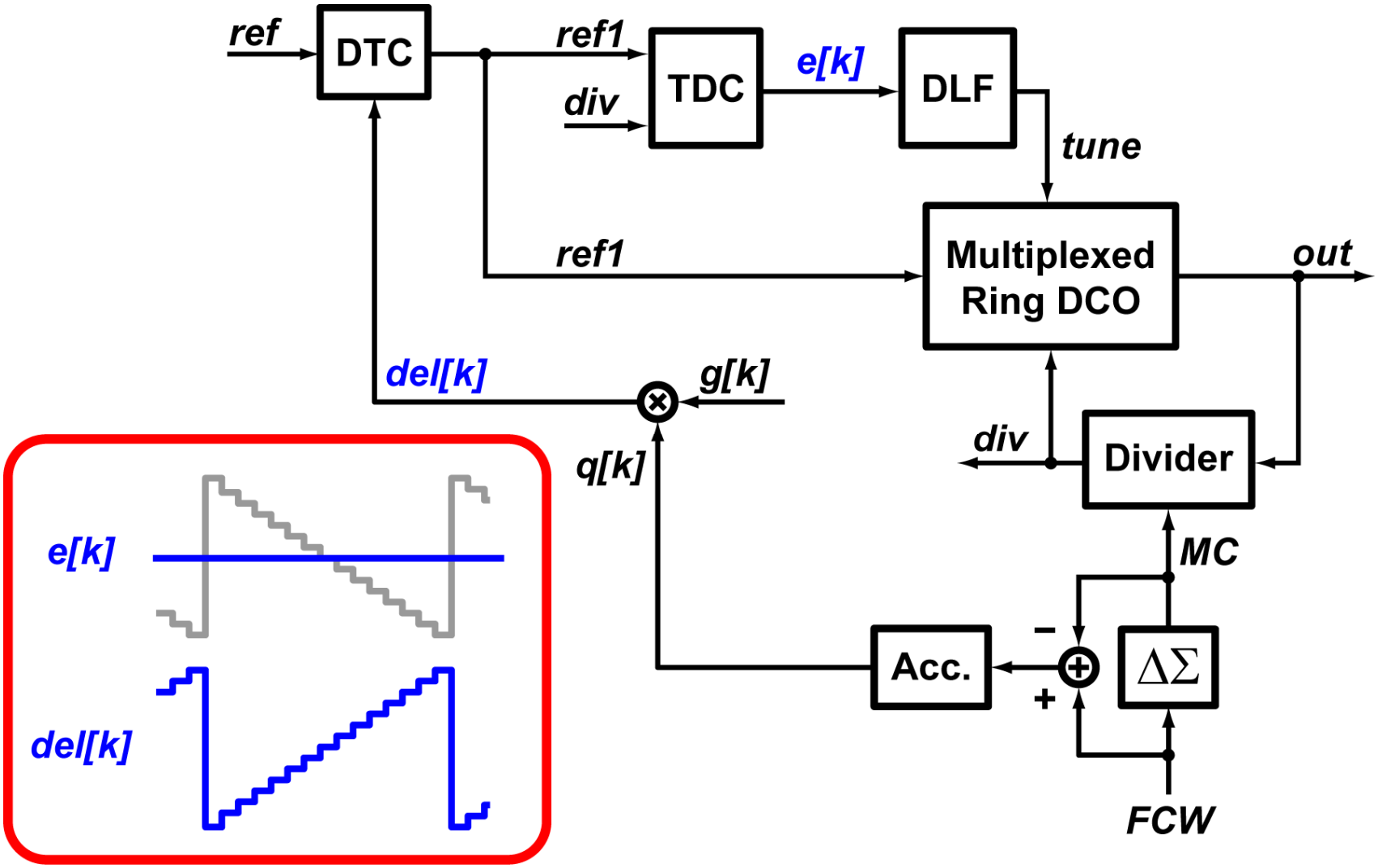
How to Control the Realignment?



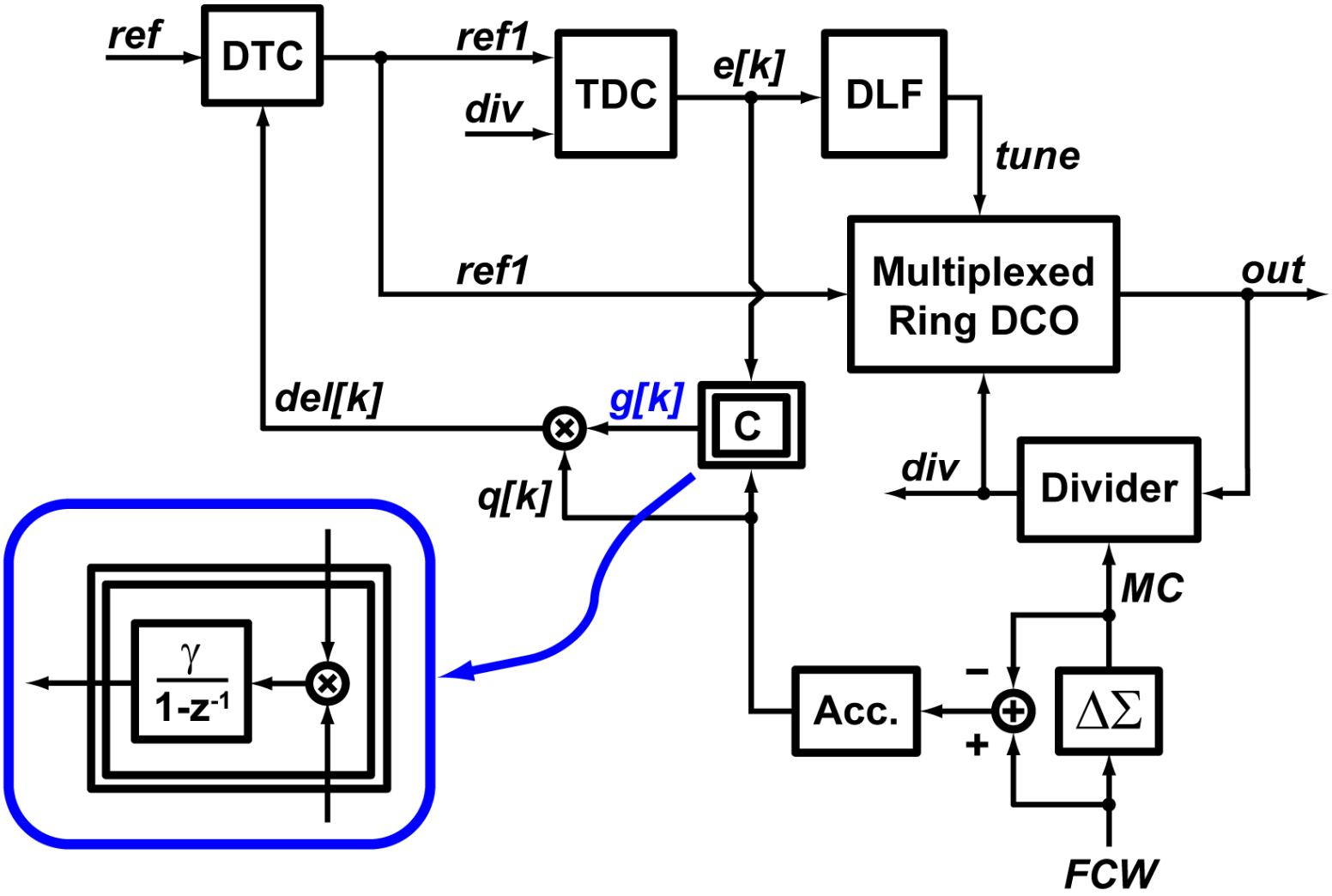
TDC Error after MC Dithering



Cancellation of TDC Error



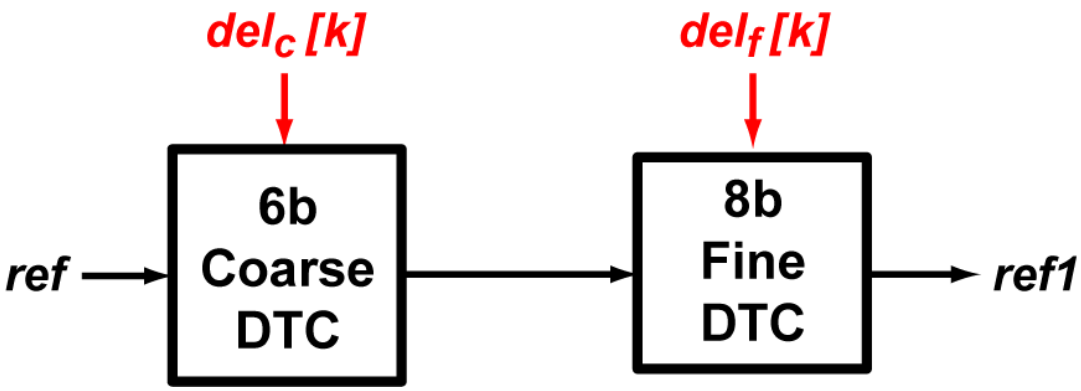
Proposed Control of Realignment



Outline

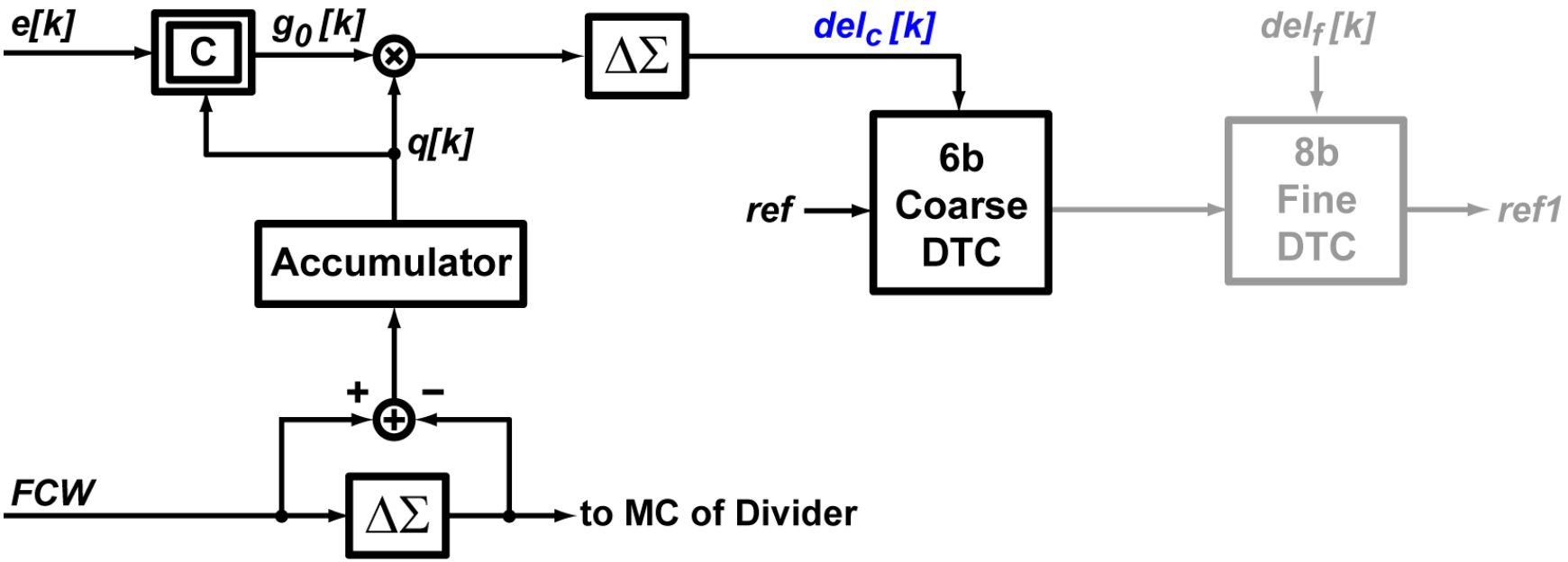
- State of the art
- Proposed architecture
- **Practical implementation**
- Measurement results
- Conclusion

Practical Implementation

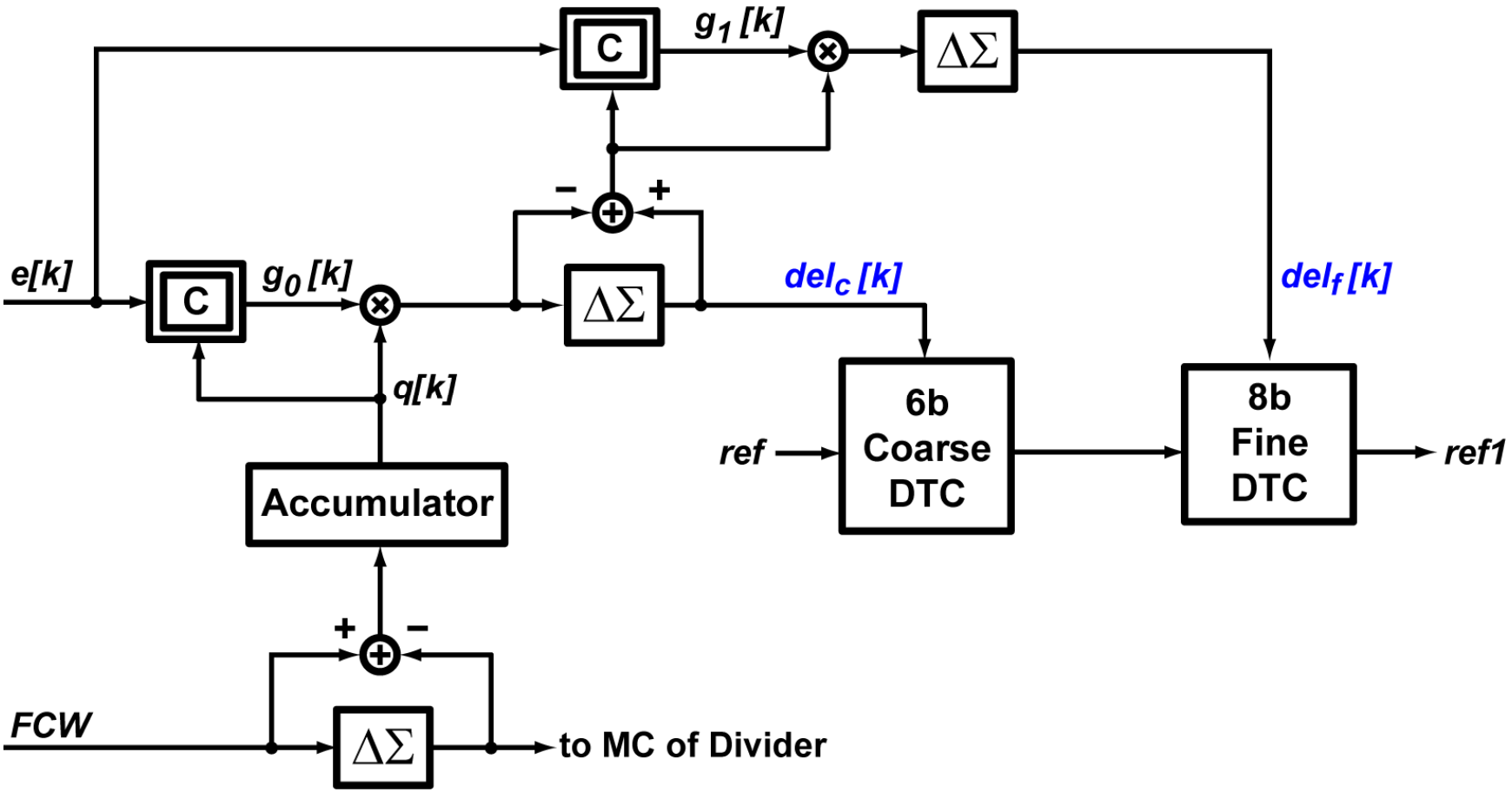


- 14b DTC pushes quantization RMS jitter below 150fs
- Segmented architecture (6b+8b) reduces area occupation to a practical value

Coarse DTC Control

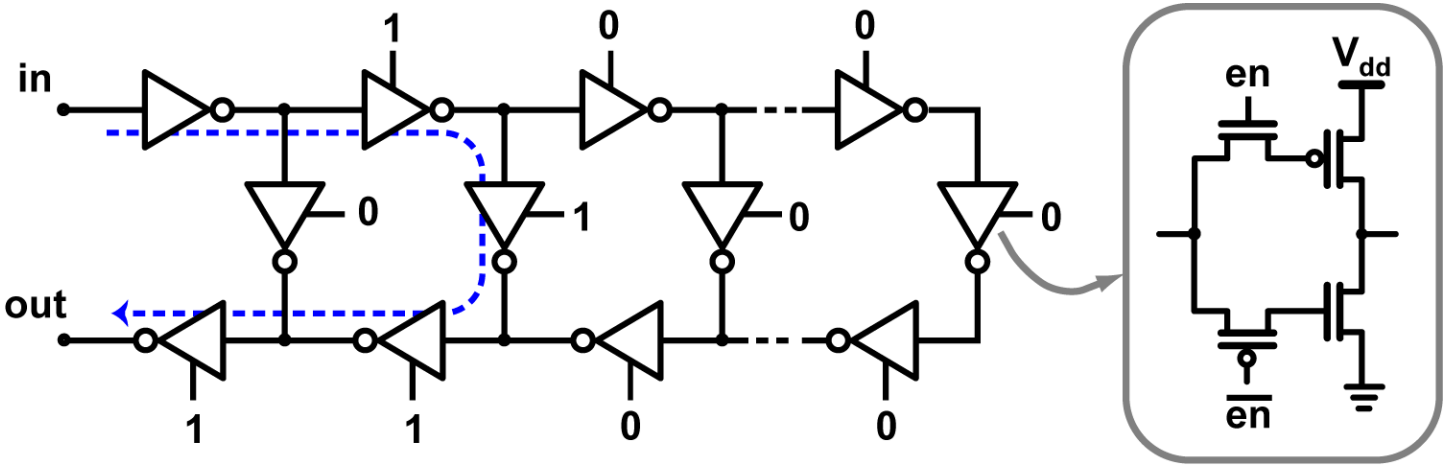


Fine DTC Control

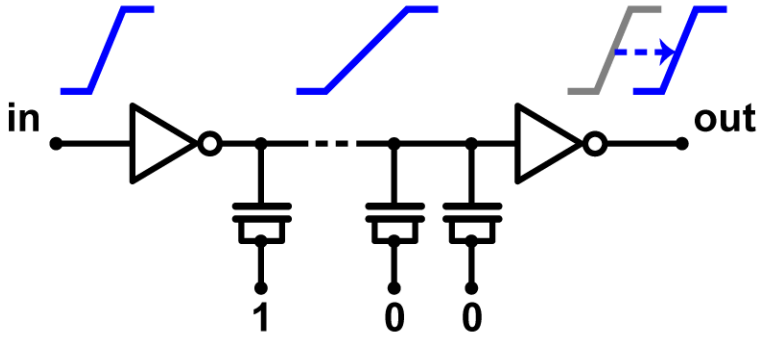


DTC Circuit Schematic

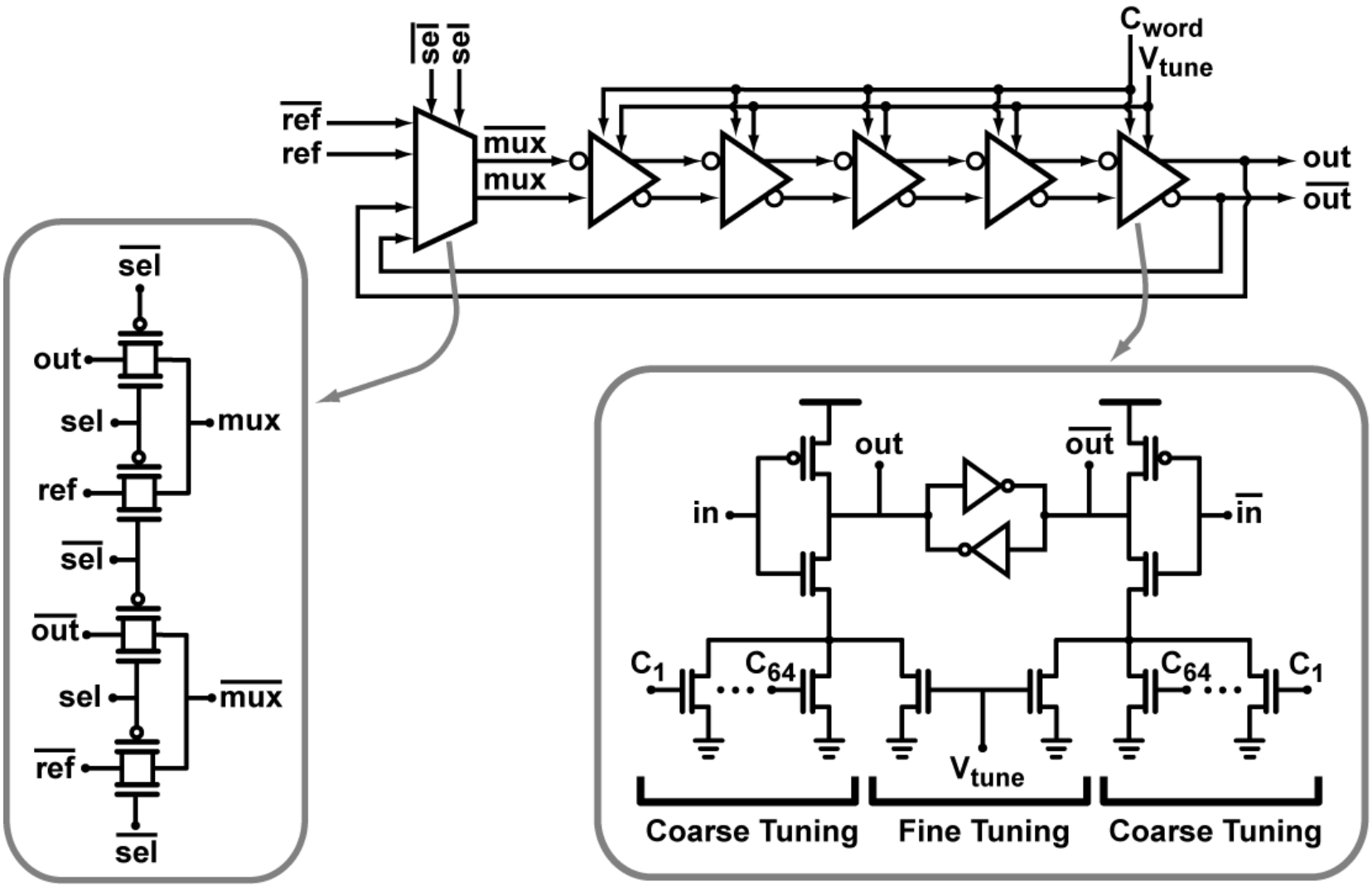
- **Coarse DTC**



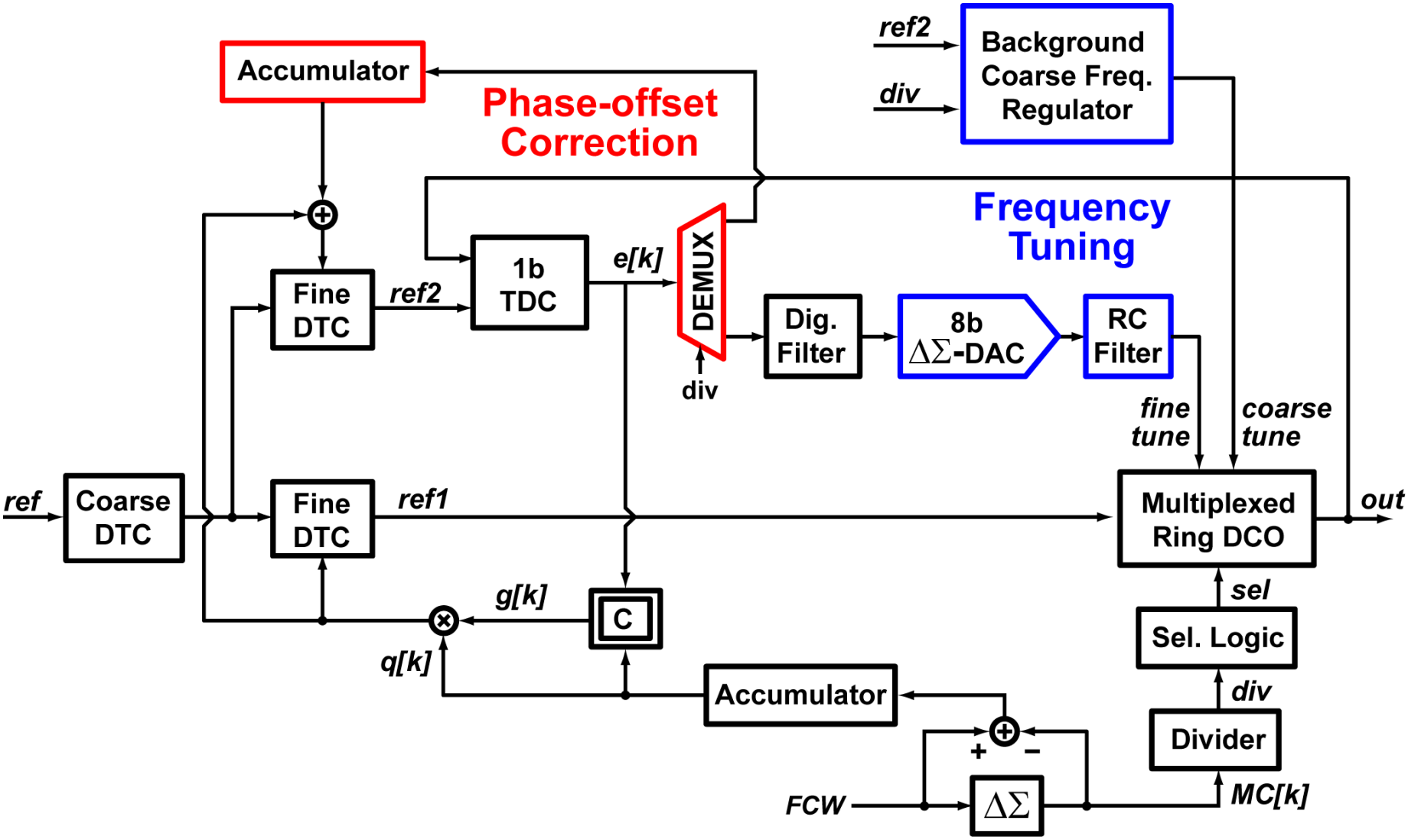
- **Fine DTC**



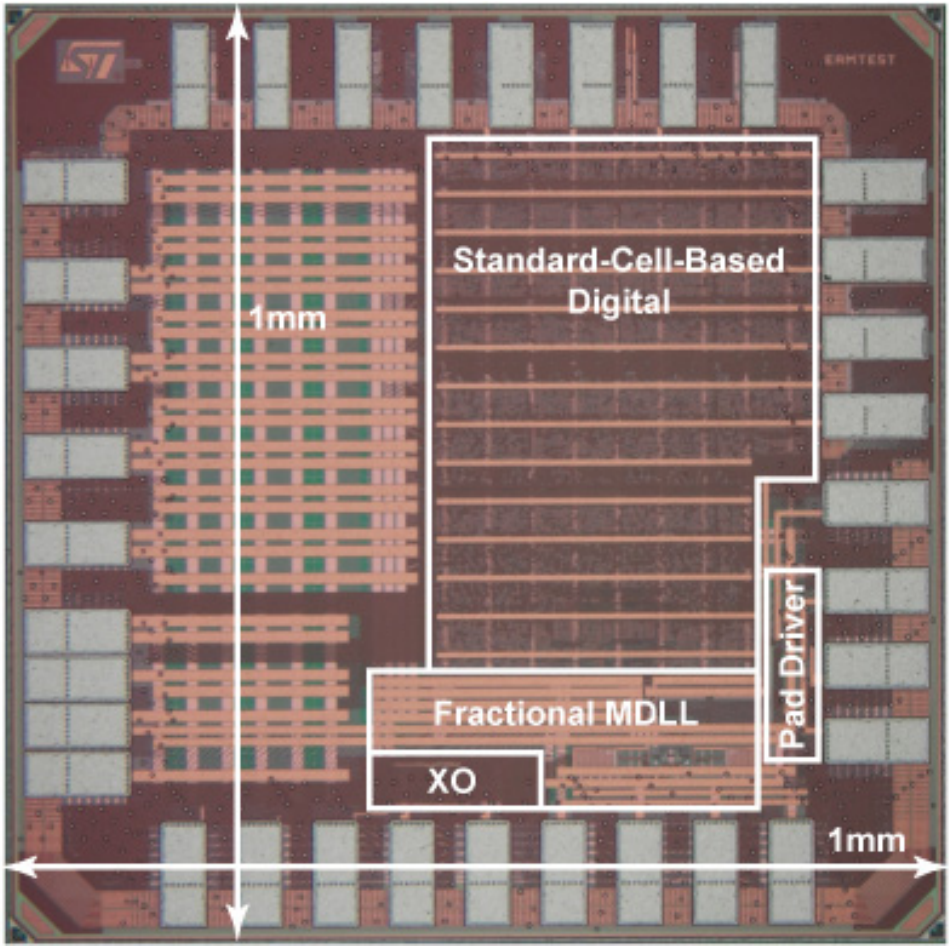
Multiplexed Ring DCO Circuit Sch.



Implemented Synthesizer (Cont'd)



Die Photograph



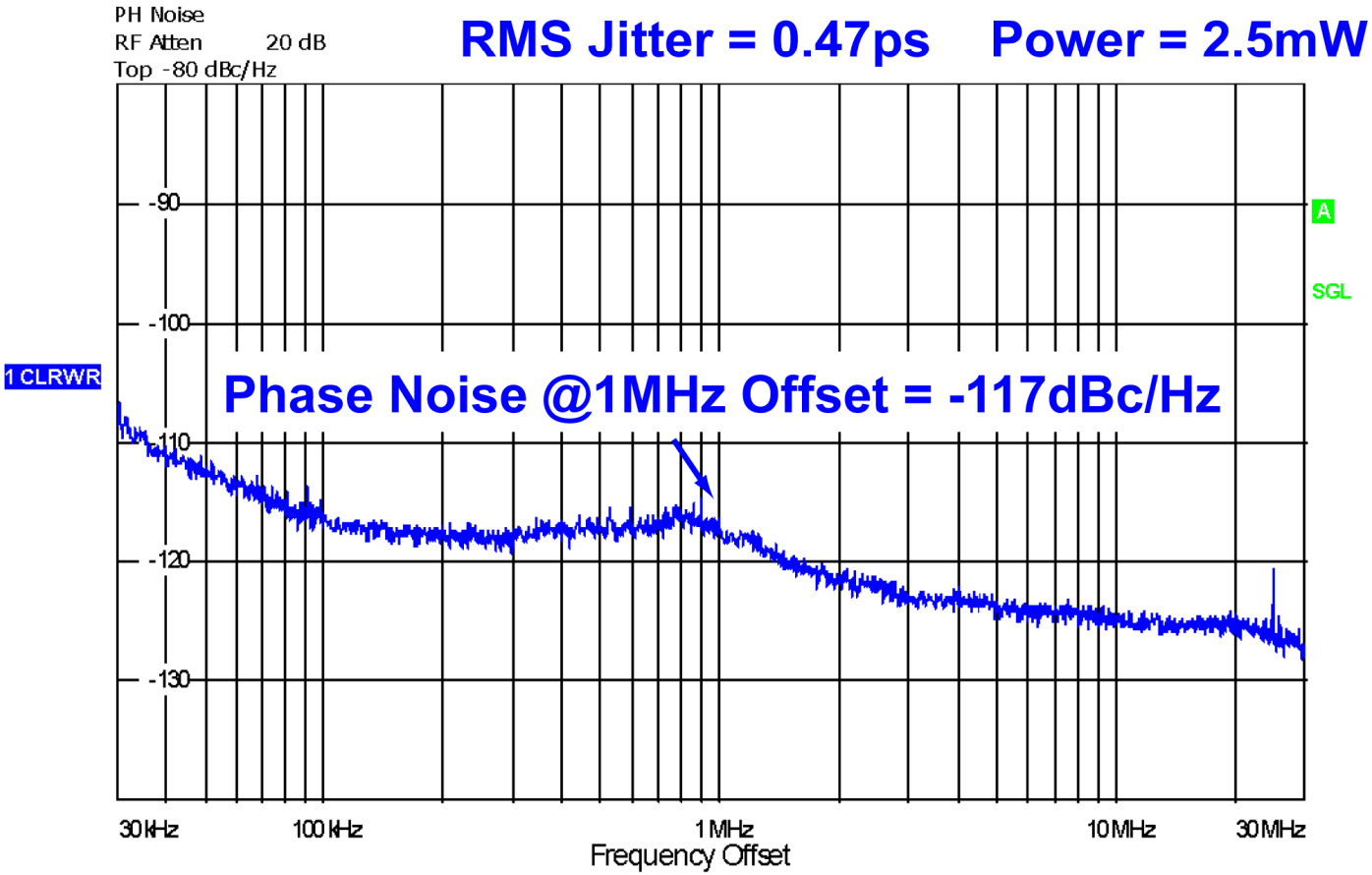
- 65nm CMOS
- 0.4mm^2 area
- 3mW power
- 1.2V supply
- 50MHz reference

Outline

- State of the art
- Proposed architecture
- Practical implementation
- **Measurement results**
- Conclusion

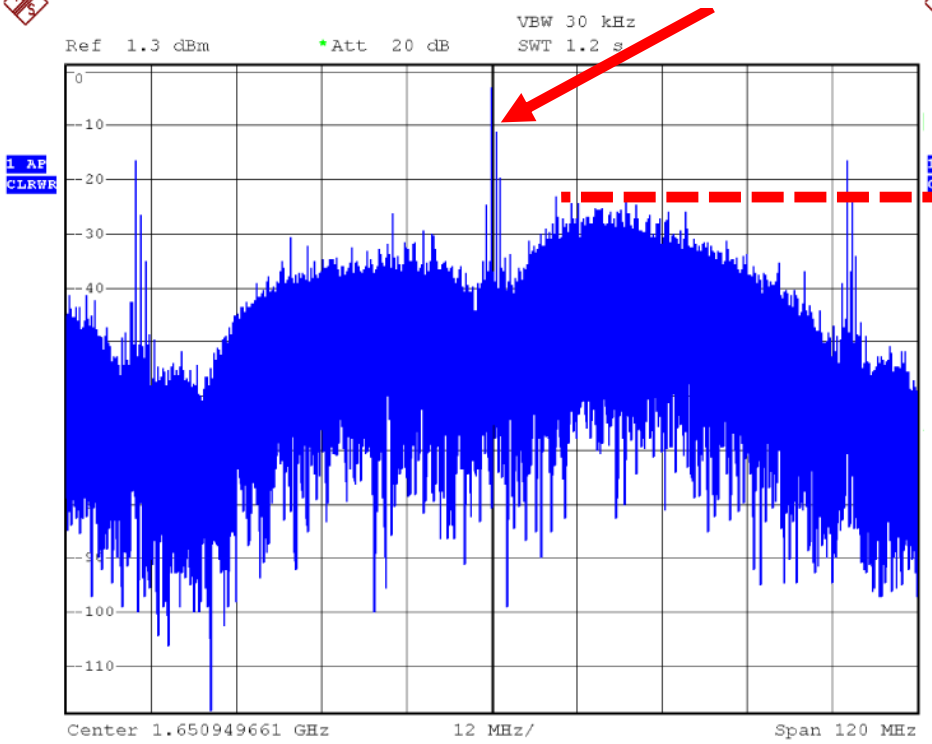
Phase Noise: Integer-N Channel

PHASE NOISE					
Settings		Residual Noise		Spot Noise [T1]	
Signal Freq:	1.600292 GHz	Evaluation from 30 kHz	to 30 MHz	30 kHz	-108.55 dBc/Hz
Signal Level:	2.61 dBm	Residual PM	0.287 °	300 kHz	-117.14 dBc/Hz
Signal Freq Δ:△	-4.2 Hz	Residual FM	69.315 kHz	3 MHz	-122.79 dBc/Hz
Signal Level Δ: △	-0.07 dBm	RMS Jitter	0.4689 ps	30 MHz	-128.11 dBc/Hz

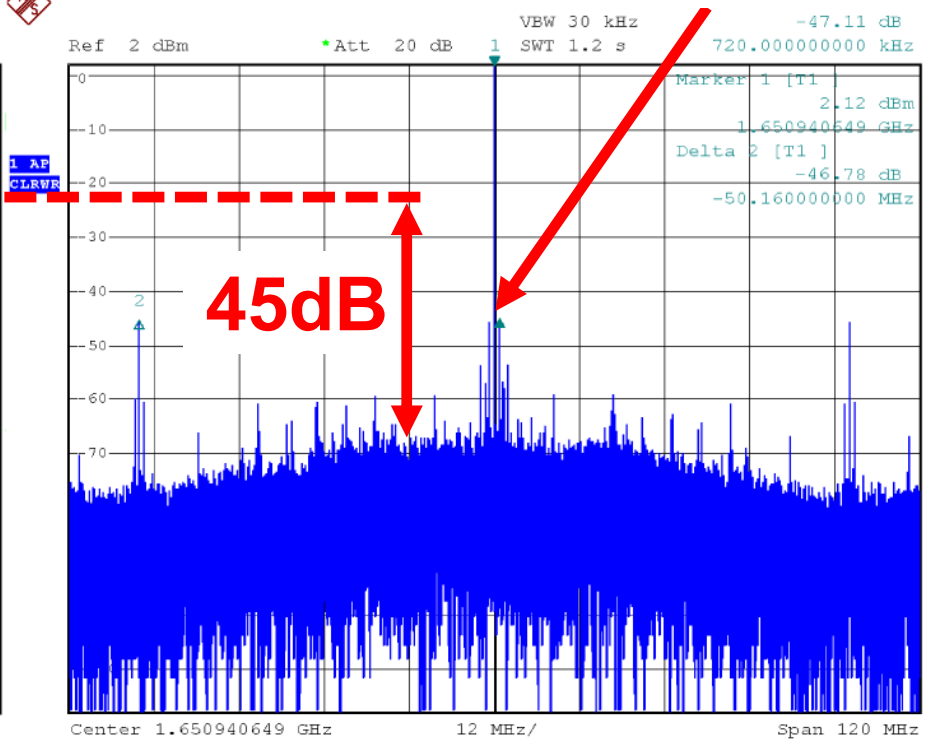


Measured Effect of Realignment

Highest spur = -12dBc



Highest spur = -47dBc



Without DTC realignment

With DTC realignment

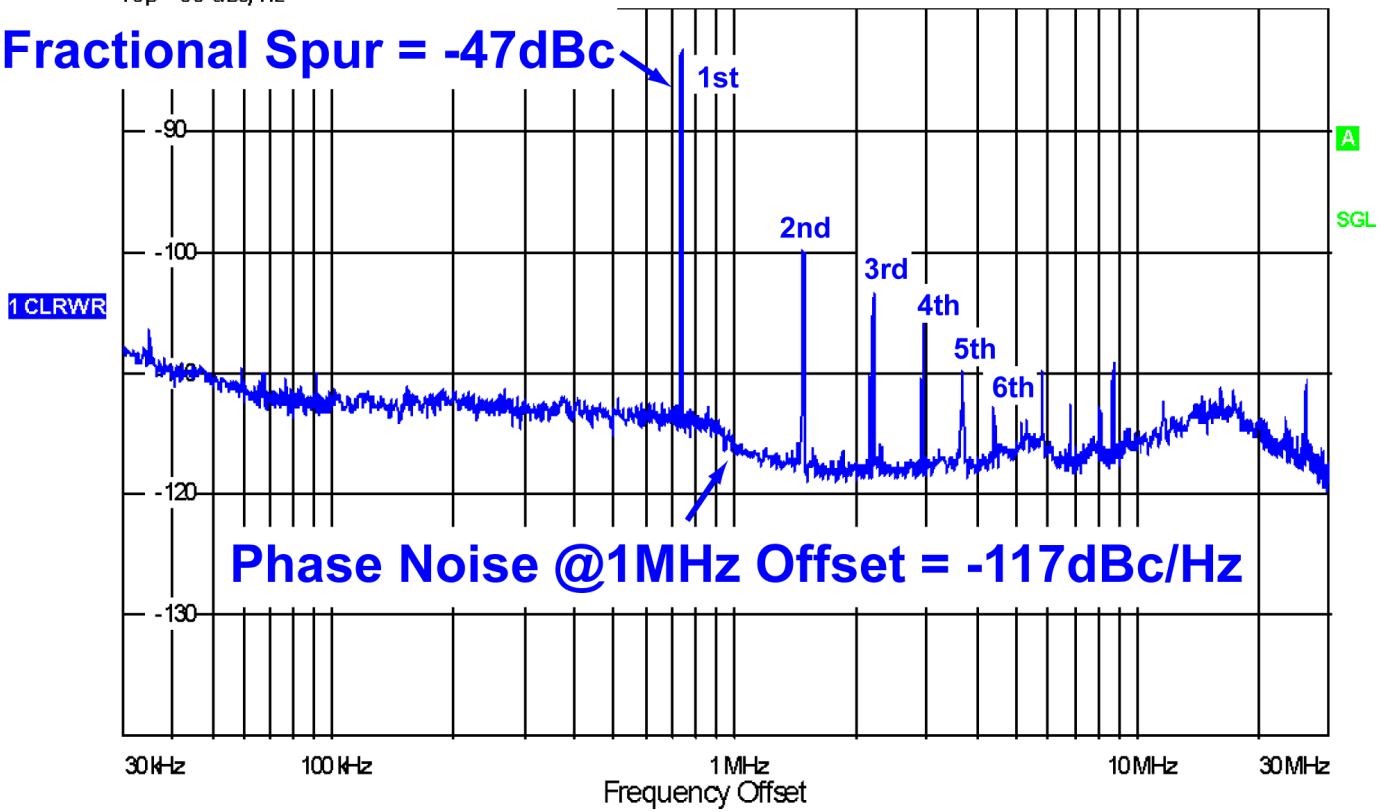
Phase Noise: Fractional-N Channel

PHASE NOISE					
Settings		Residual Noise		Spot Noise [T1]	
Signal Freq:	1.651041 GHz	Evaluation from 30 kHz	to 30 MHz	100 kHz	-112.07 dBc/Hz
Signal Level:	2.19 dBm	Residual PM	0.829 °	1 MHz	-116.69 dBc/Hz
Signal Freq Δ:△	29.54 Hz	Residual FM	246.053 kHz	10 MHz	-114.96 dBc/Hz
Signal Level Δ: △	-0.01 dBm	RMS Jitter	1.3953 ps	30 MHz	-117.65 dBc/Hz

PH Noise
RF Atten 20 dB
Top -80 dBc/Hz

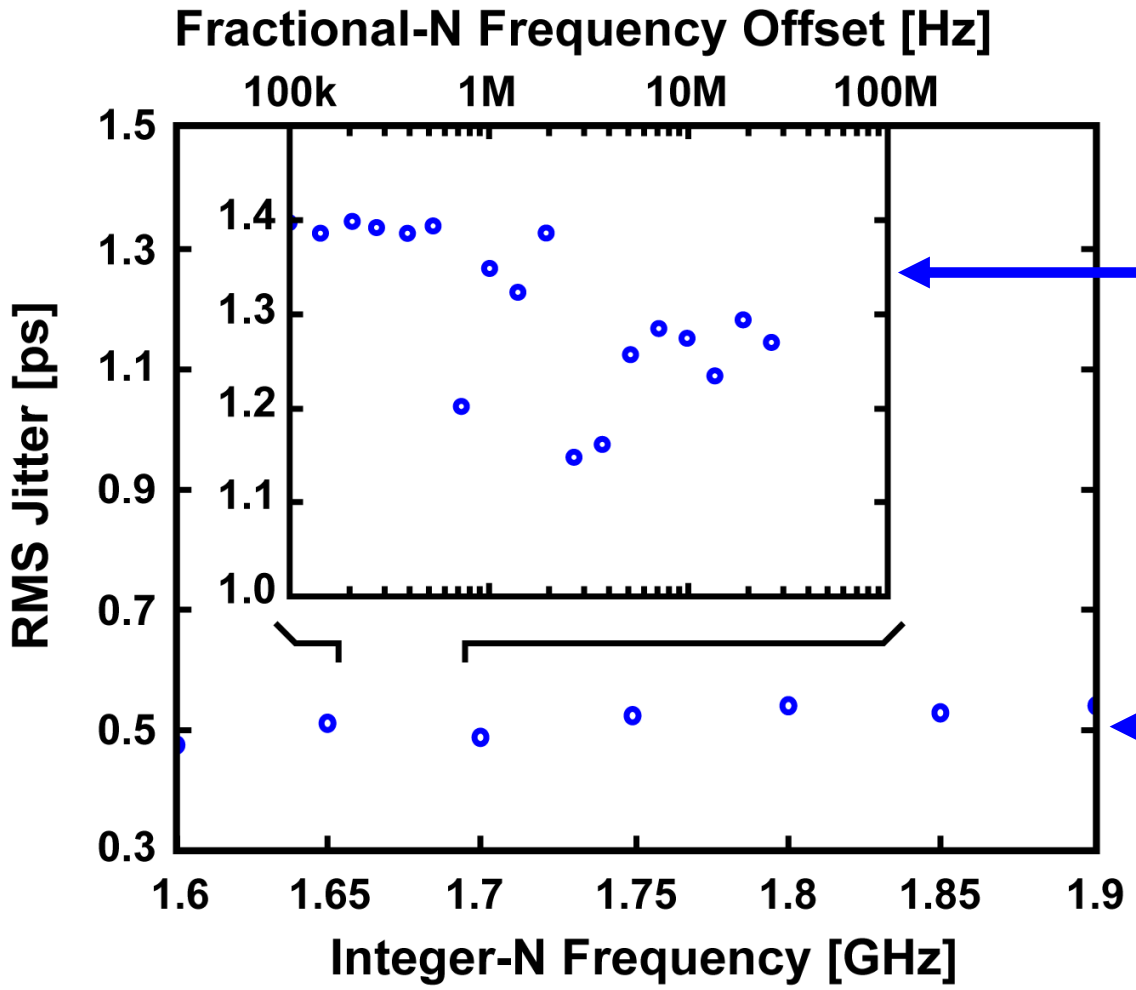
RMS Jitter = 1.4ps **Power = 3mW**

In-band Fractional Spur = -47dBc



Phase Noise @1MHz Offset = -117dBc/Hz

Measured Jitter Over Channels



Fract.-N RMS jitter < 1.4ps

Integer-N RMS jitter < 550fs

- **Integrated RMS jitter (30kHz-30MHz)**

Performance Comparison Table

	This Work	[4] P. Park ISSCC12	S. Lee RFIC12
Architecture	IL-PLL	IL-PLL	IL-PLL
Frequency Resolution (kHz)	0.19	1000	40000
Reference Frequency (MHz)	50	32	80
Output Frequency (GHz)	1.6 - 1.9	0.58	1.8
Reference Spur (dBc)	-47 (-55)*	N/A	-35
Near Integer Frac. Spur (dBc)	-47 (720kHz)	N/A	N/A
Far Integer Frac. Spur (dBc)	-51 (2MHz)	N/A	N/A
Integ. RMS Jitter (ps)	1.4	8	N/A
Power Dissipation (mW)	3	10.1	22
Area occupation (mm^2)	0.4	0.158	0.083
CMOS Process (nm)	65	65	90

* Off-chip reference signal generator

Conclusion

- **Fine-resolution fractional-N frequency synthesizer with an injection-locked inductor-less oscillator**
- **Our DTC-based architecture with background gain regulation cancels the fractional quantization error**

1.7GHz Frequency Synthesizer

with 190Hz Resolution,

1.4ps RMS Jitter, 3mW Power

Acknowledgement

- **The authors wish to thank M. Zuffada and E. Temporiti of STMicroelectronics for supporting chip fabrication**

21.2
A 2.3-GHz Fractional-N Divider-less Phase-Locked Loop with -112dBc/Hz In-Band Phase Noise

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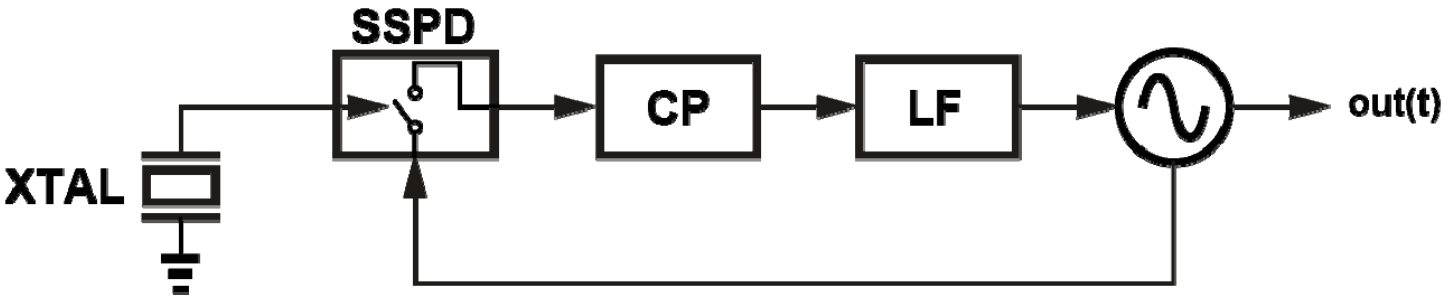
Taipei, Taiwan, R.O.C

Outline

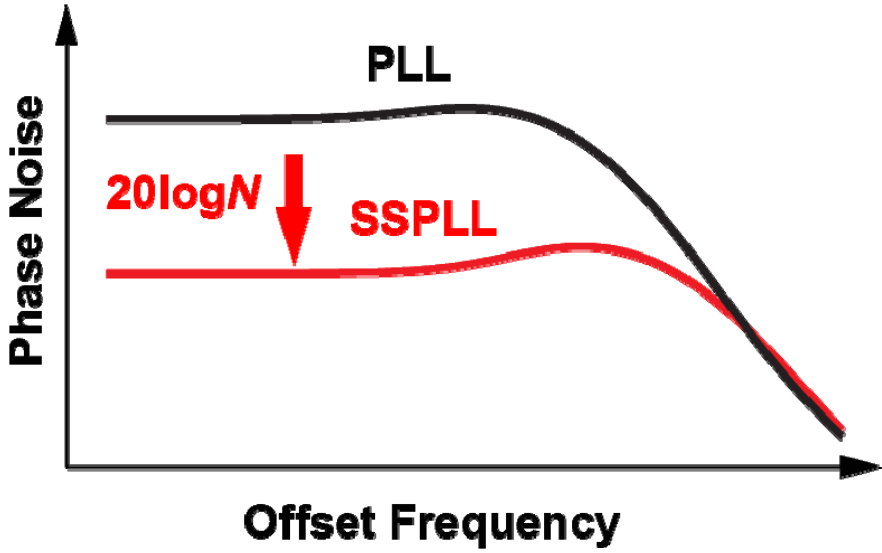
- Background
- Fractional-N divider-less PLL
- Digital pulse-width modulator (DPWM)
- Implementation
- Measurement Results
- Conclusions

Background

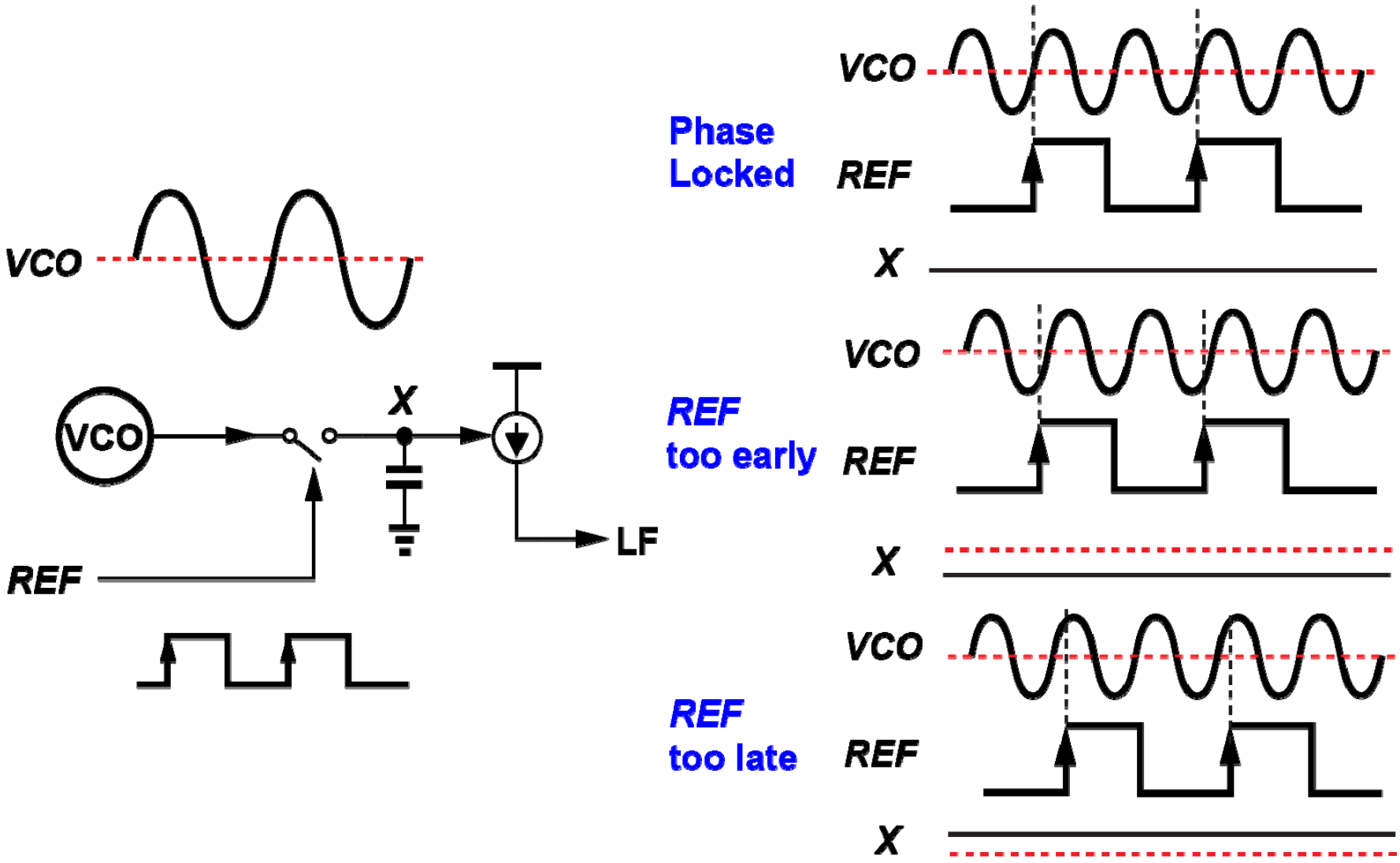


[Gao, ISSCC 09]

- Sub-Sampling based PLL
- Very low in-band phase noise
  - PD/CP noise not multiplied by N^2
  - No divider noise and power



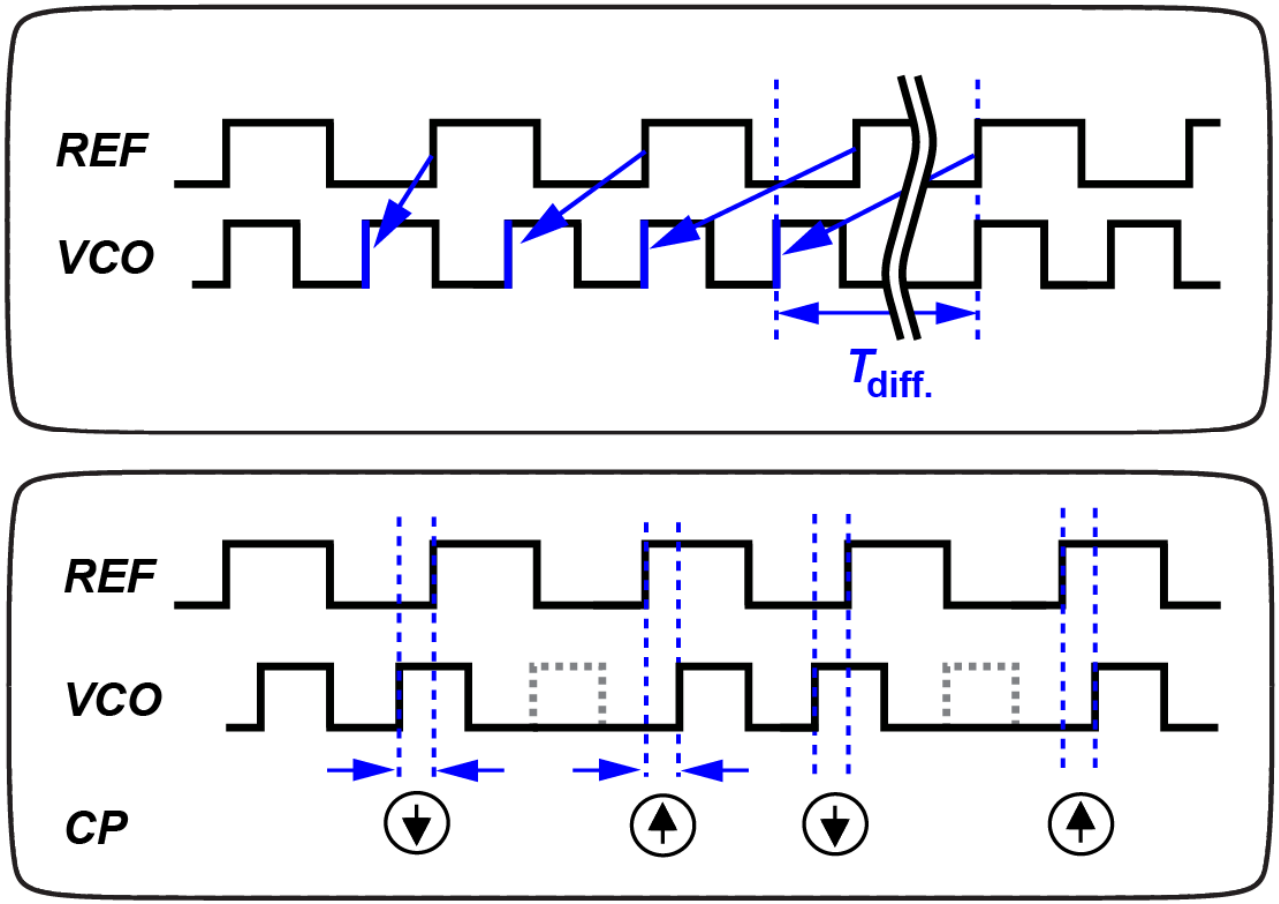
SSPLL Characteristic



- SSPLL can only operate in integer-N mode

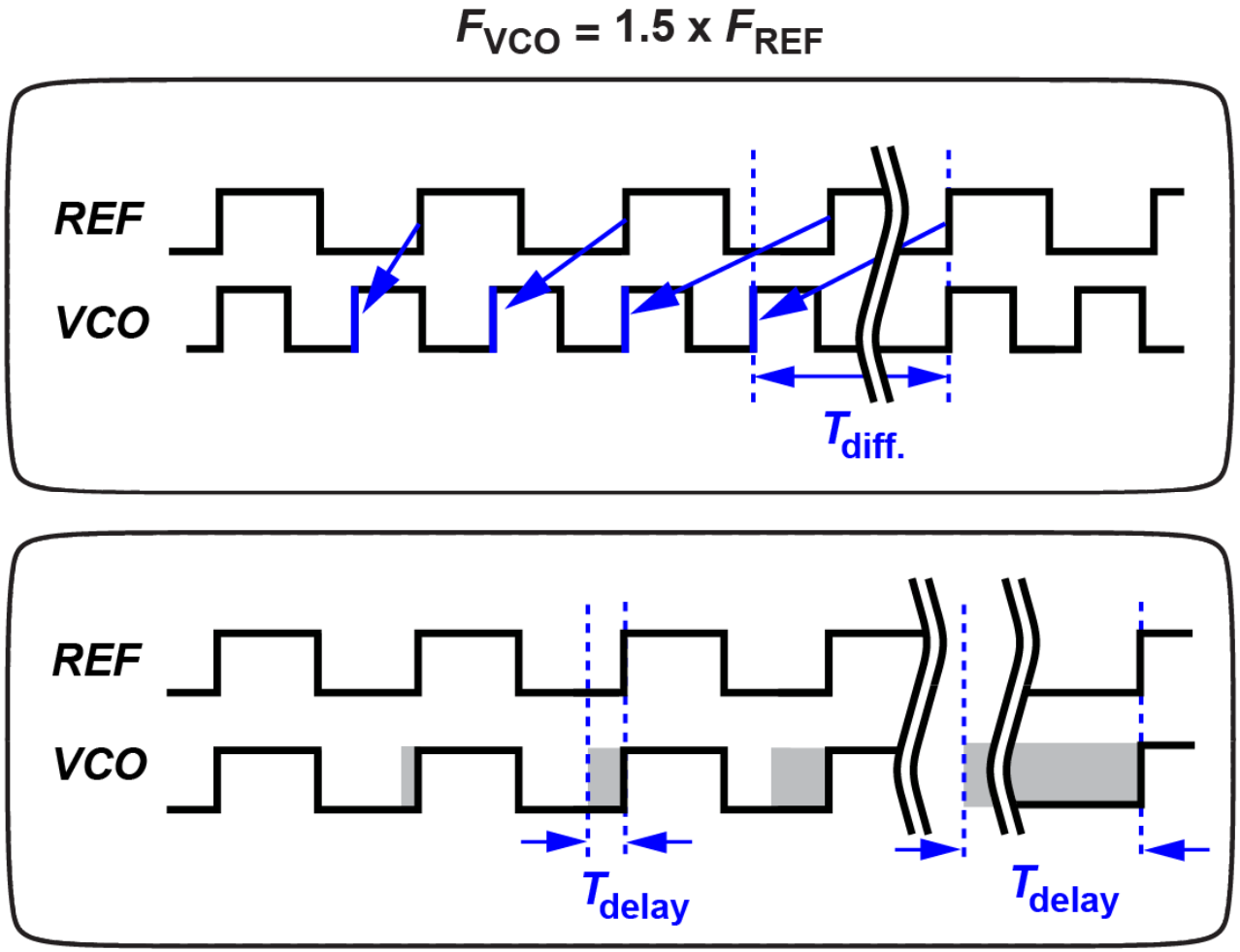
Fractional-N Operation (I)

$F_{VCO} = 1.5 \times F_{REF}$



- **Programmable divider required**

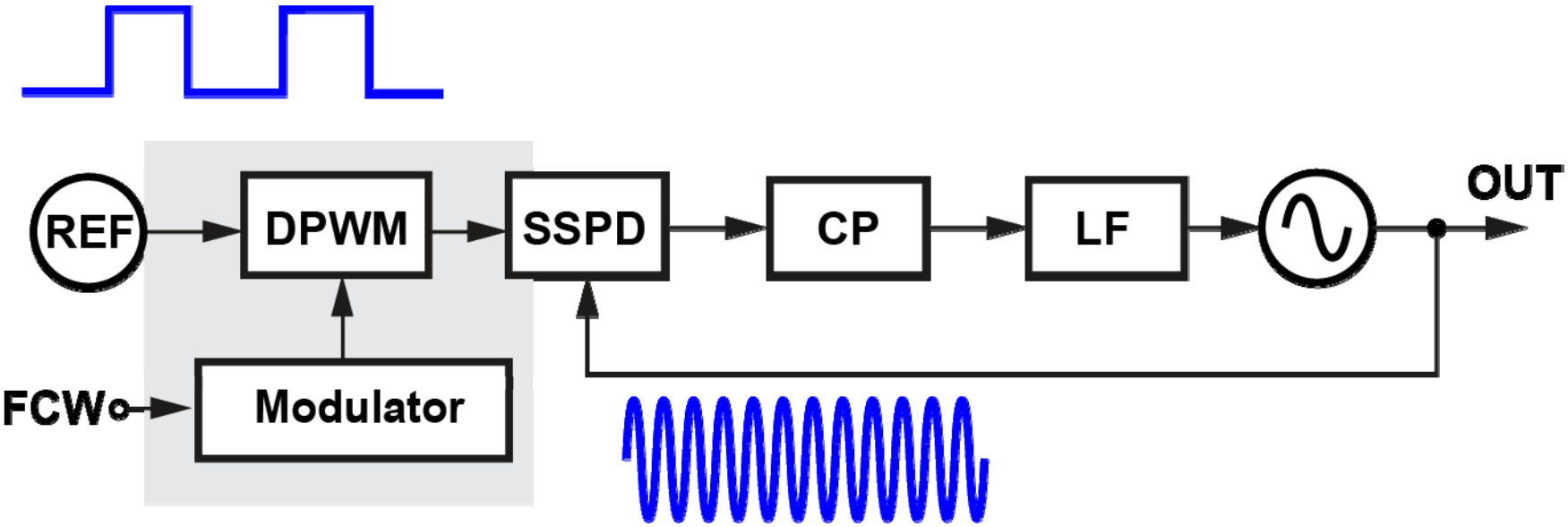
Fractional-N Operation (II)



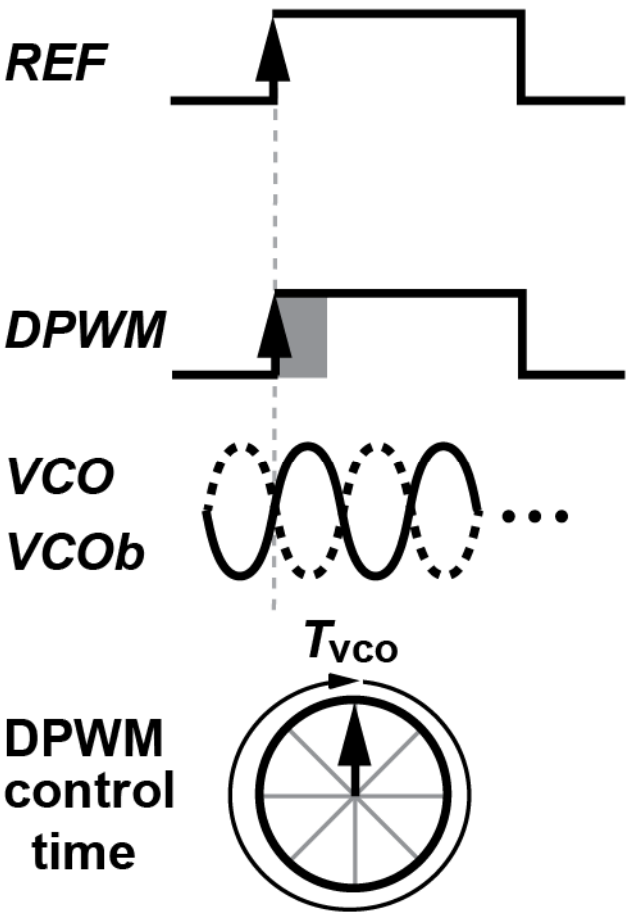
- **Programmable infinite delay required**

Can we use the SSPLL in fractional-N mode ?

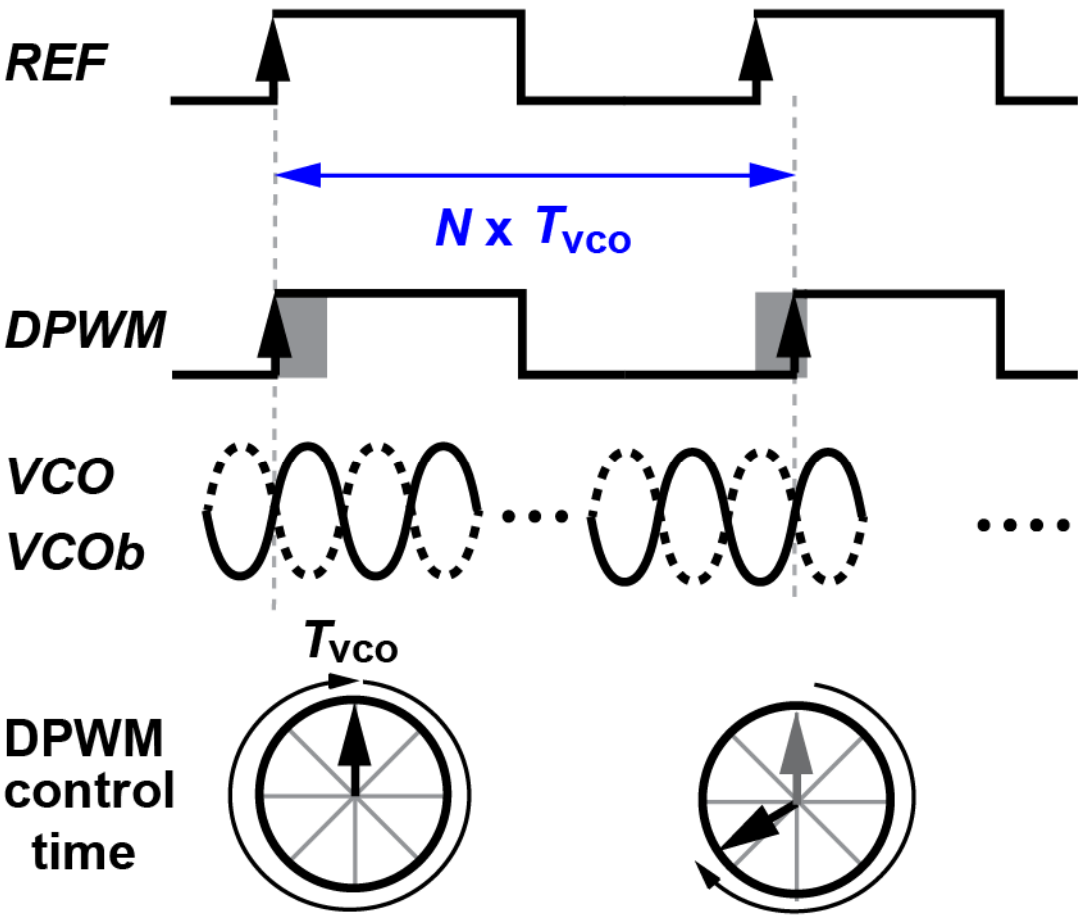
Proposed Architecture



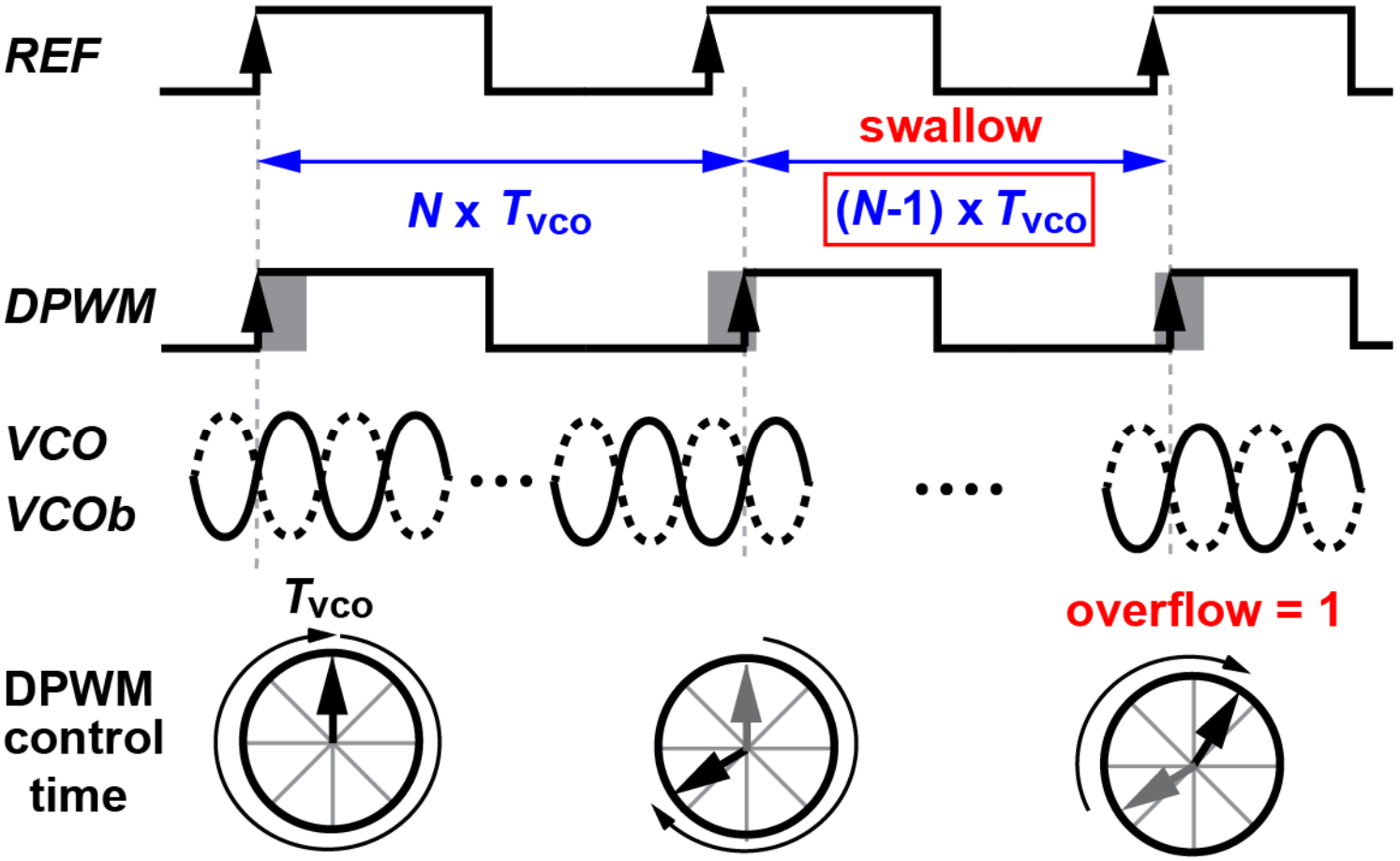
Fractional-N Operation



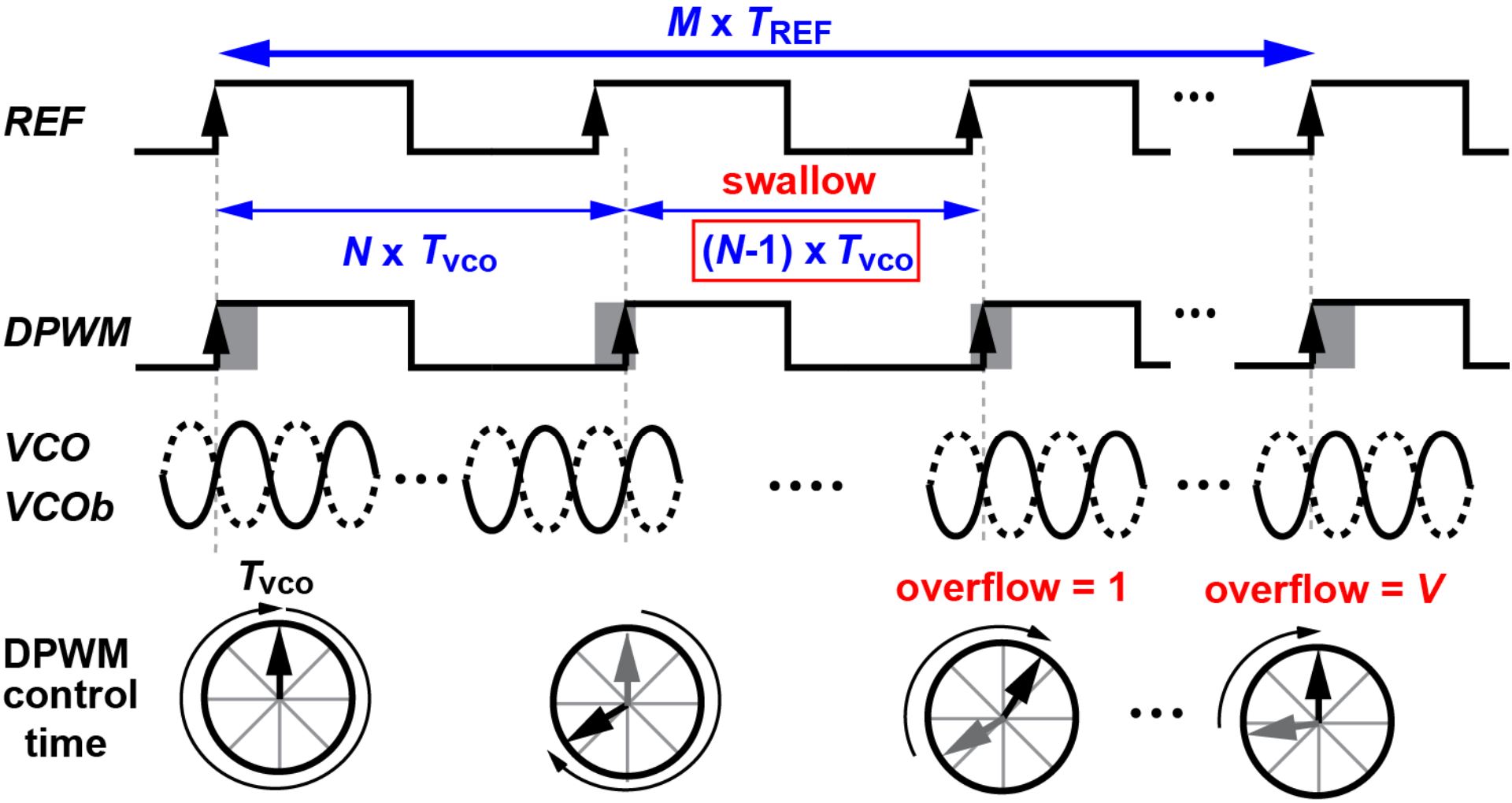
Fractional-N Operation



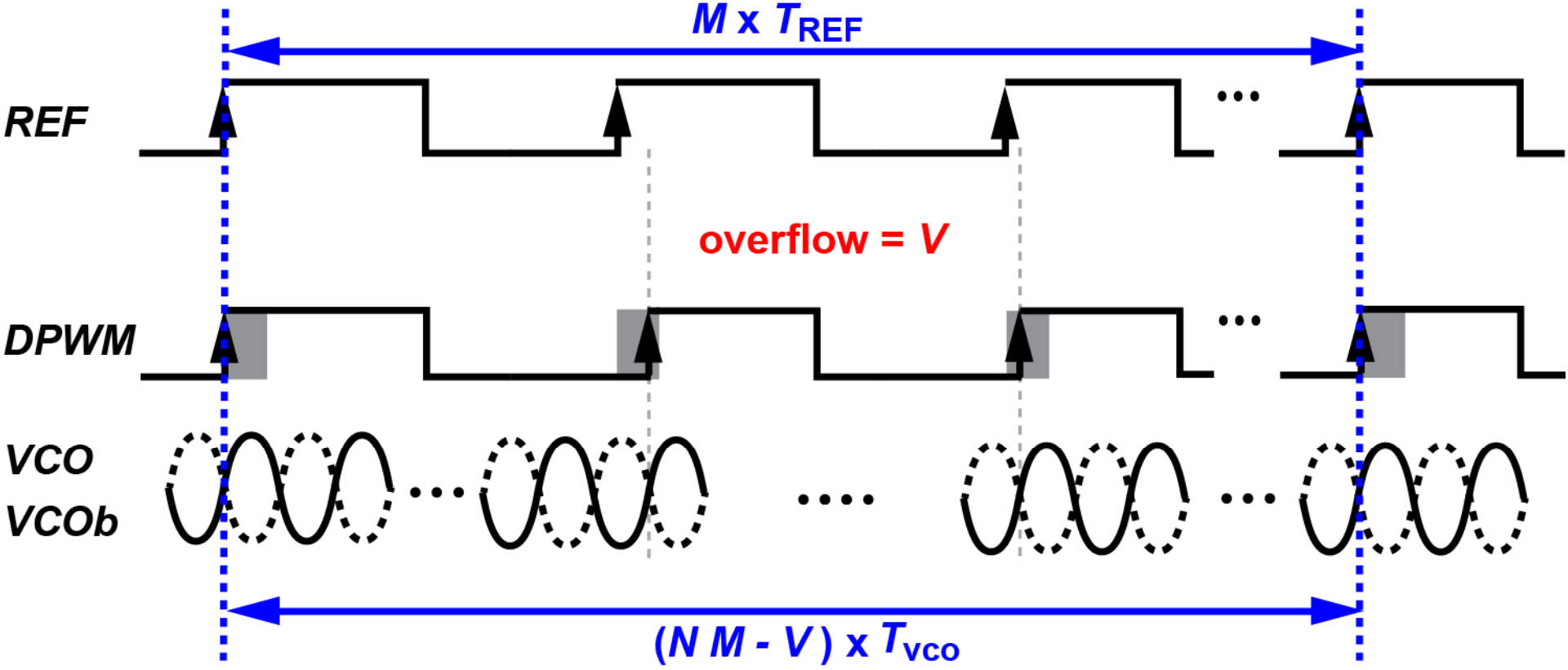
Fractional-N Operation



Fractional-N Operation

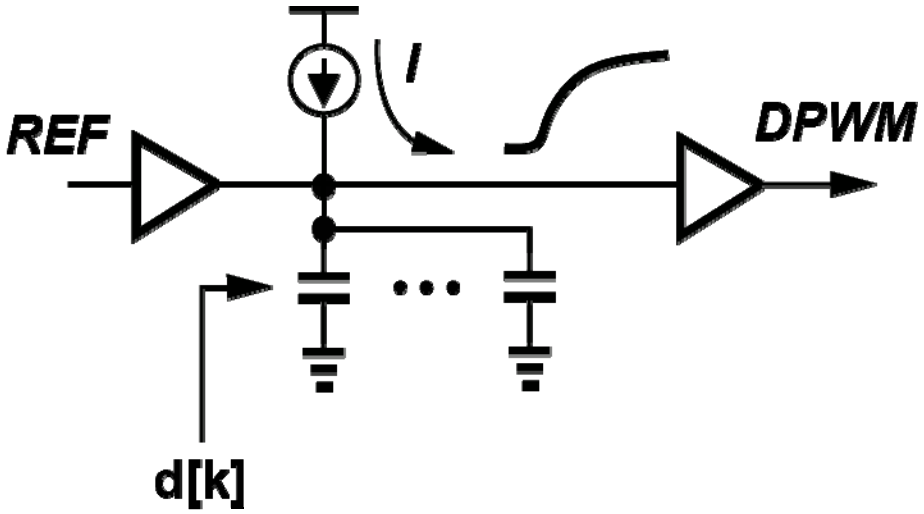


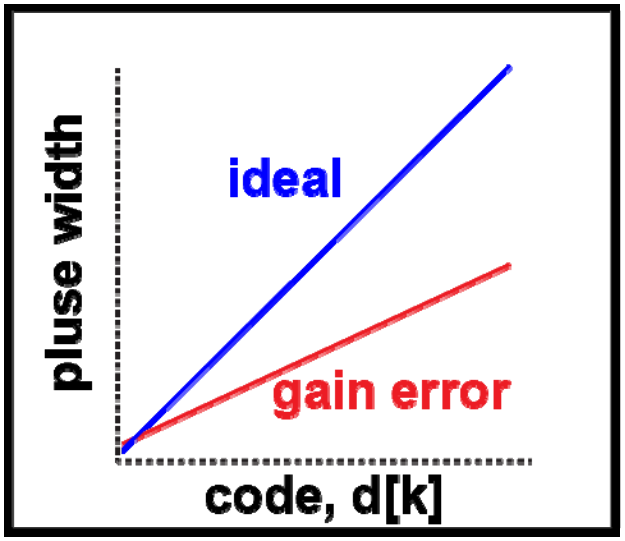
Fractional-N Operation

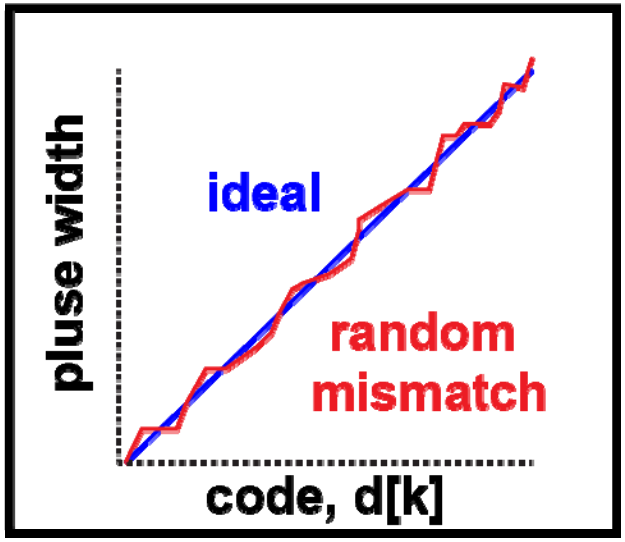


- **Swallow-divider-like operation without dividers**

DPWM Implementation





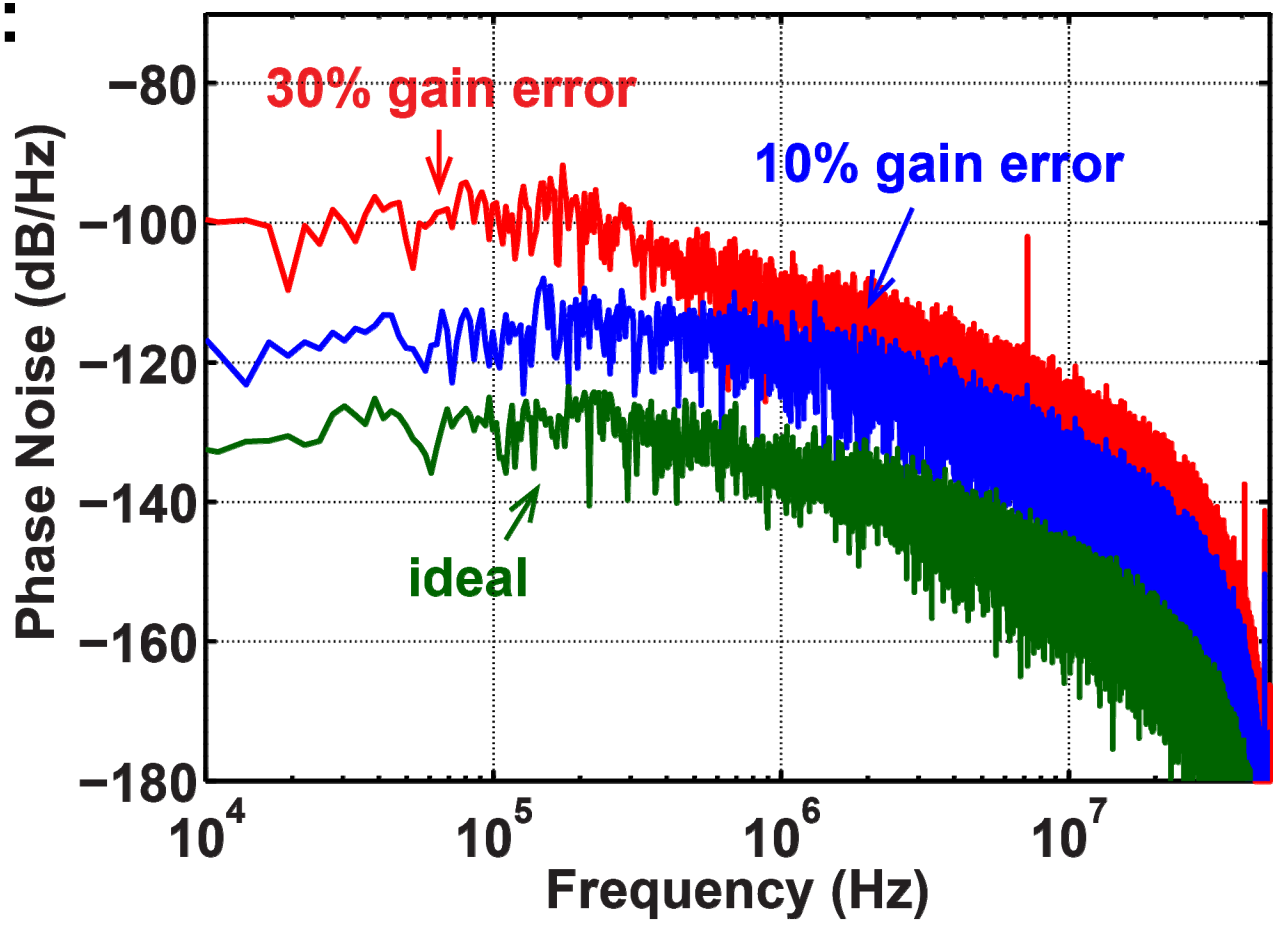


Two important sources of errors

- **Gain error**
- **Random mismatch**

DPWM Non-Ideal Effect

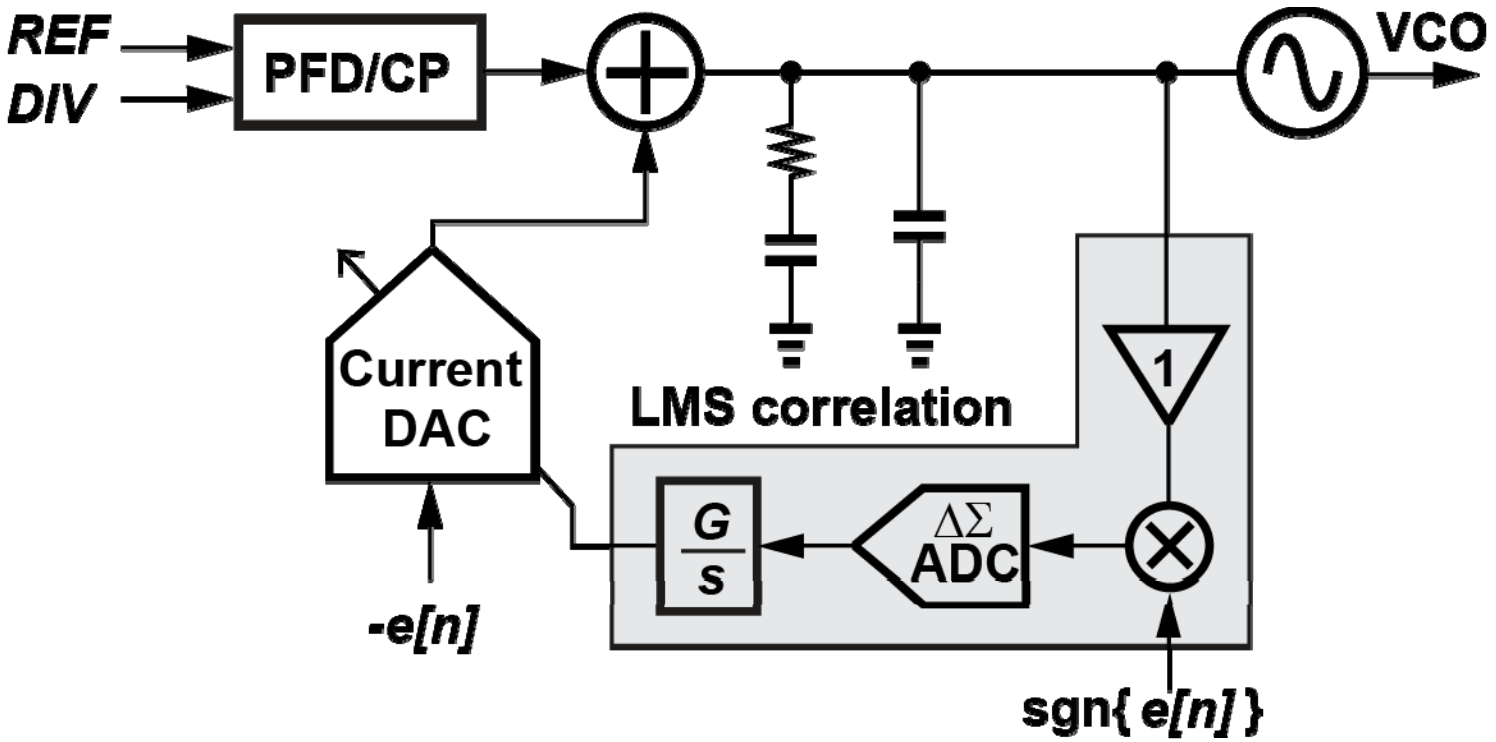
- In all cases, CP has 5% current mismatch.
- Gain error:



- Random mismatch: raise in-band noise

How to resolve the gain error of the DPWM?

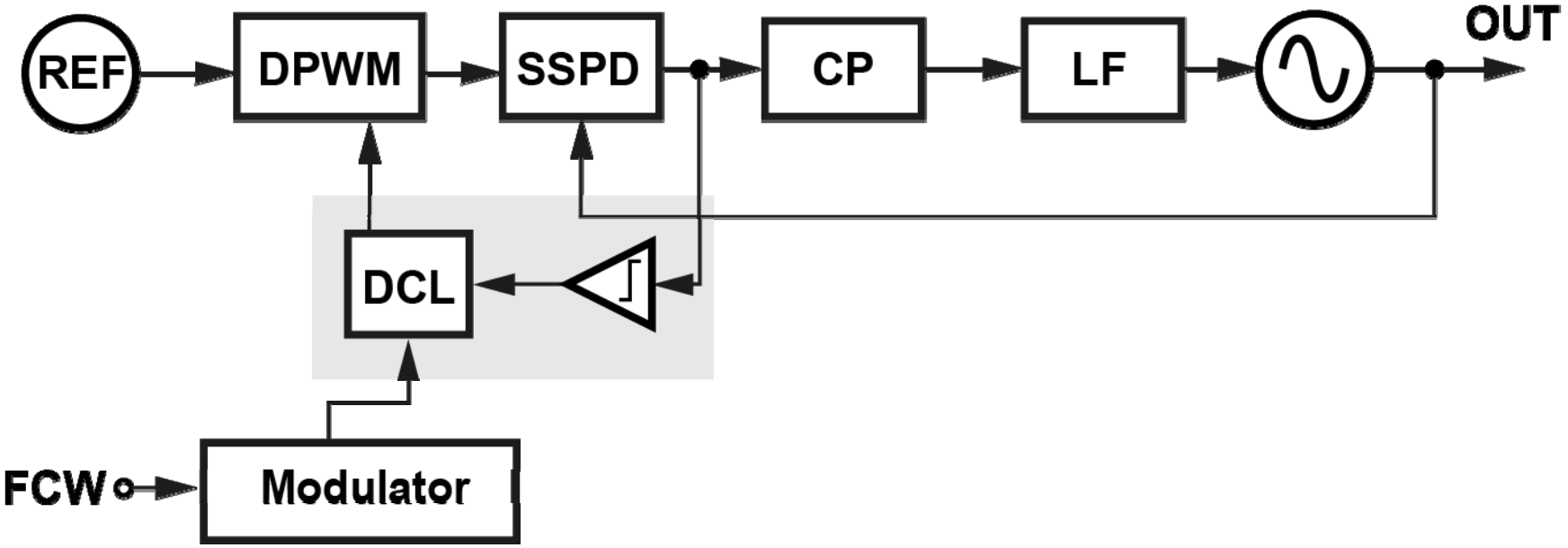
Previously Work of LMS Correlation



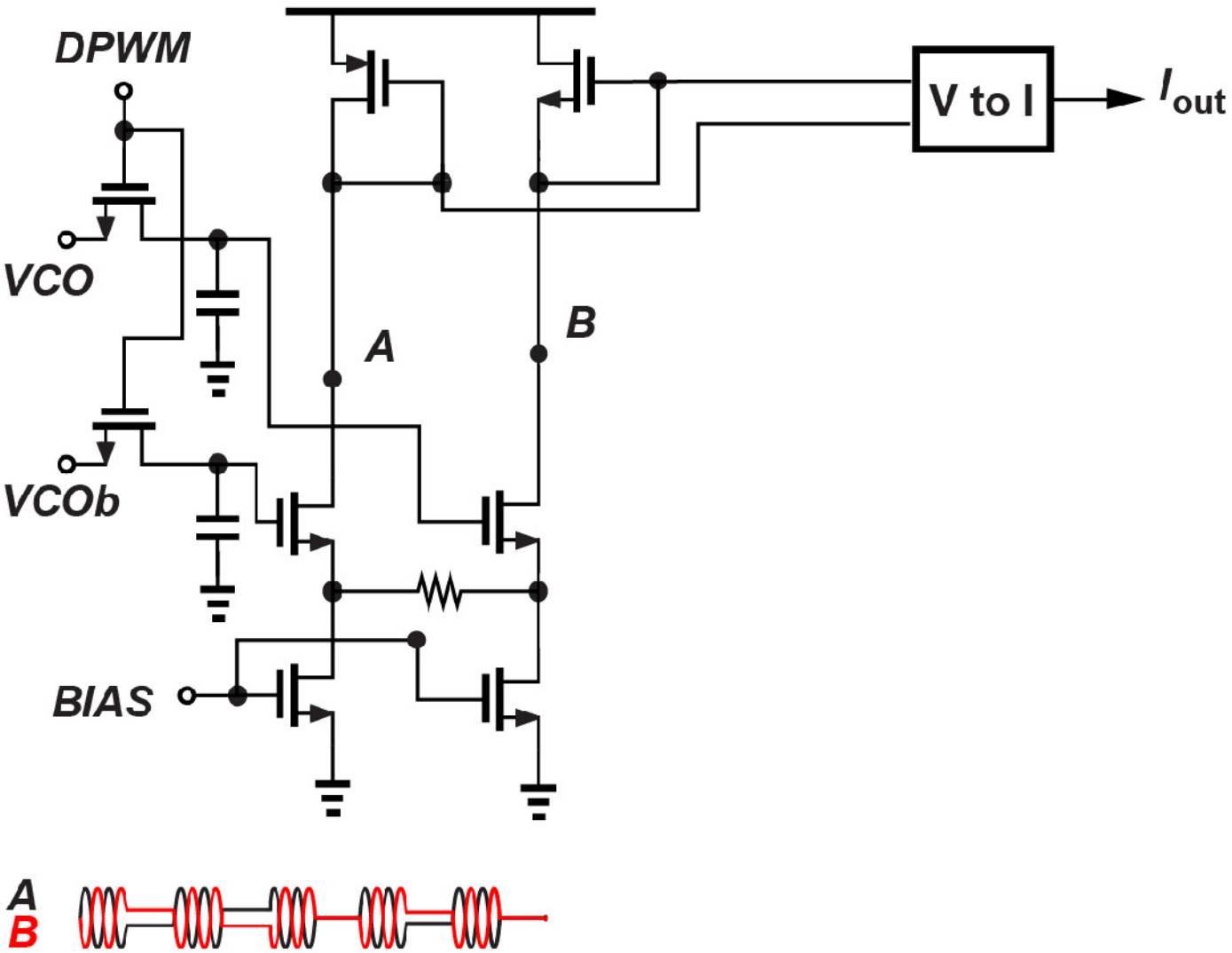
[Gupta, ISSCC 06]

- A ΔΣ ADC with high dynamic range is required.

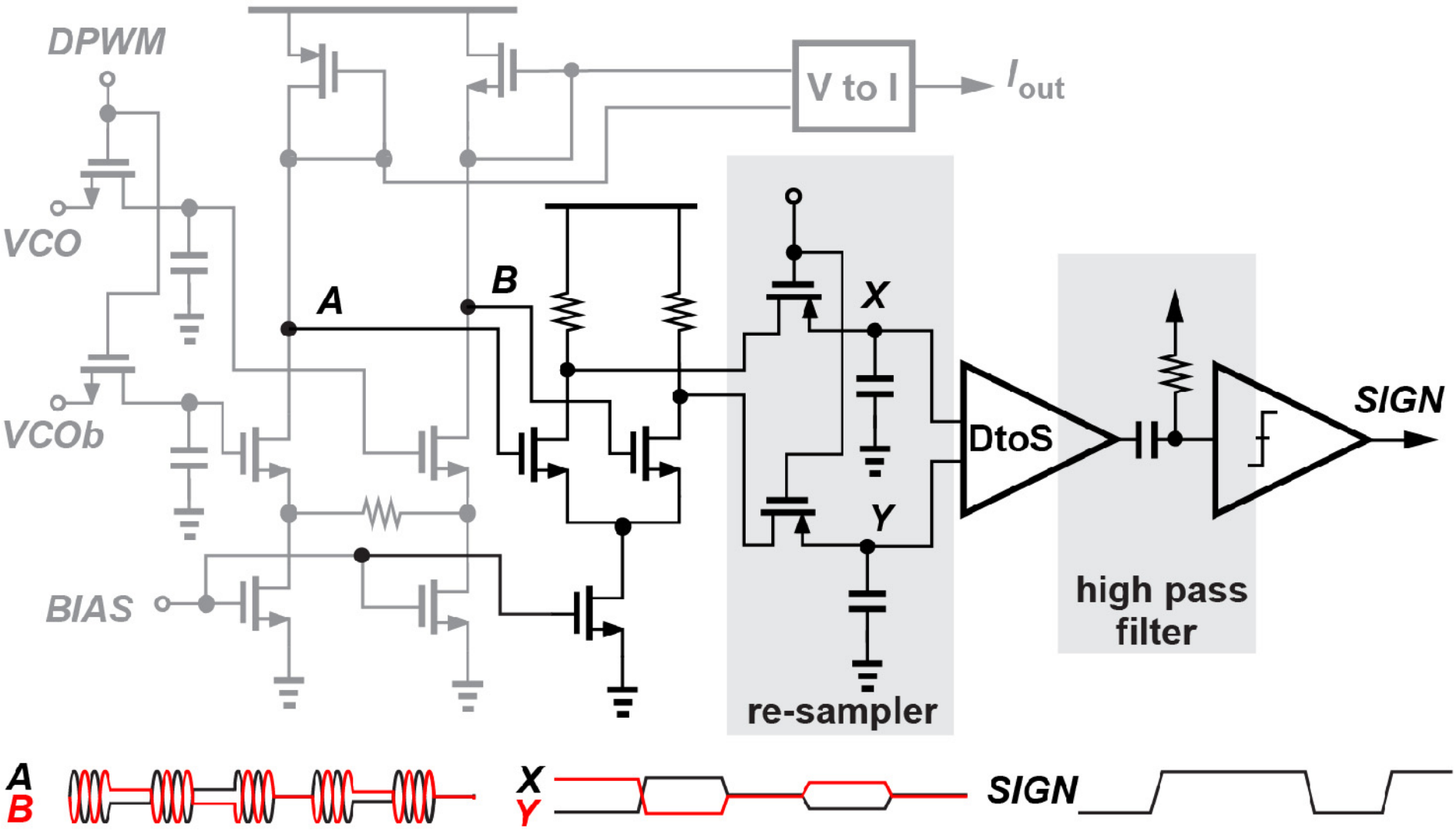
Proposed Architecture



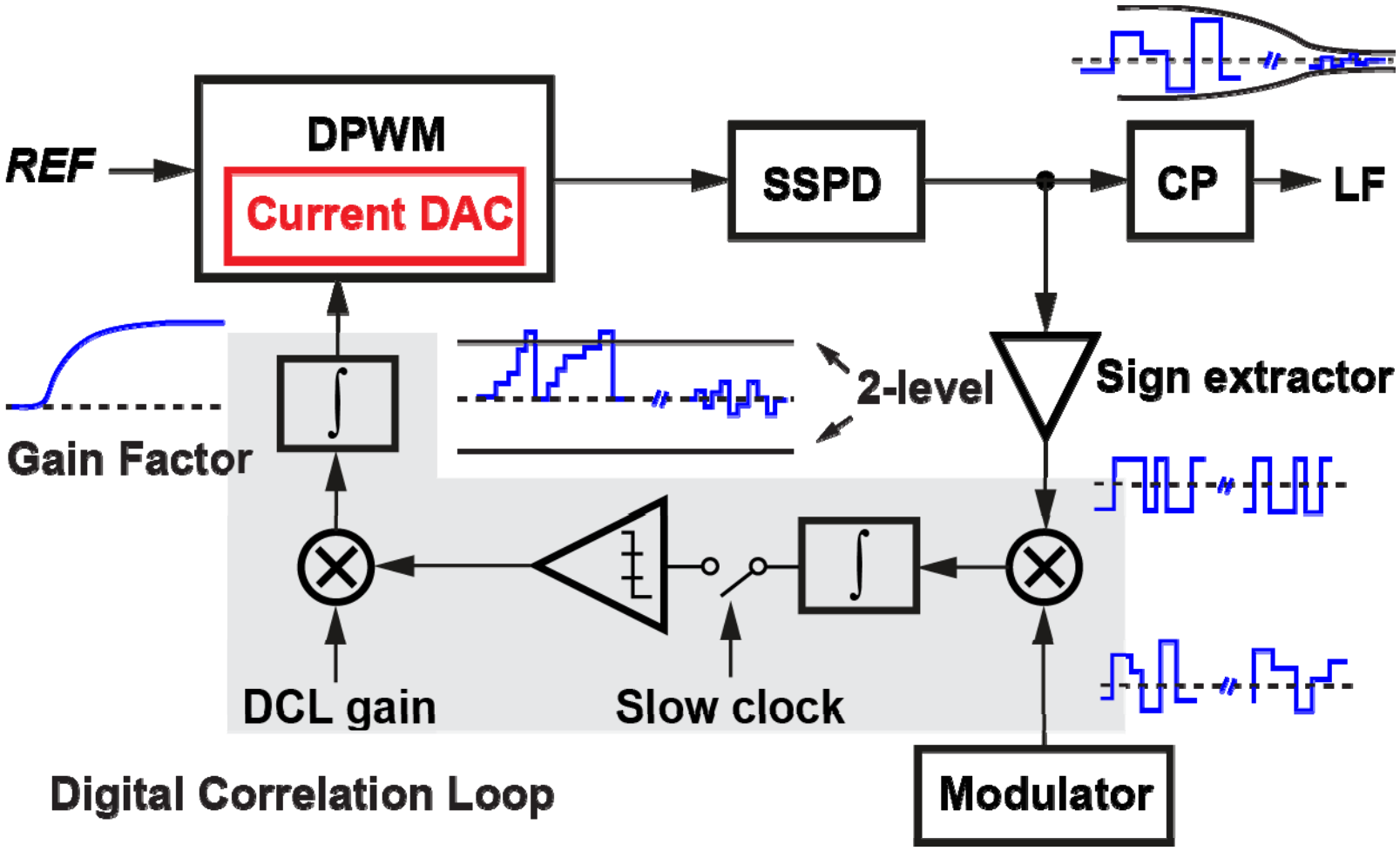
SSPD



Sign Extractor

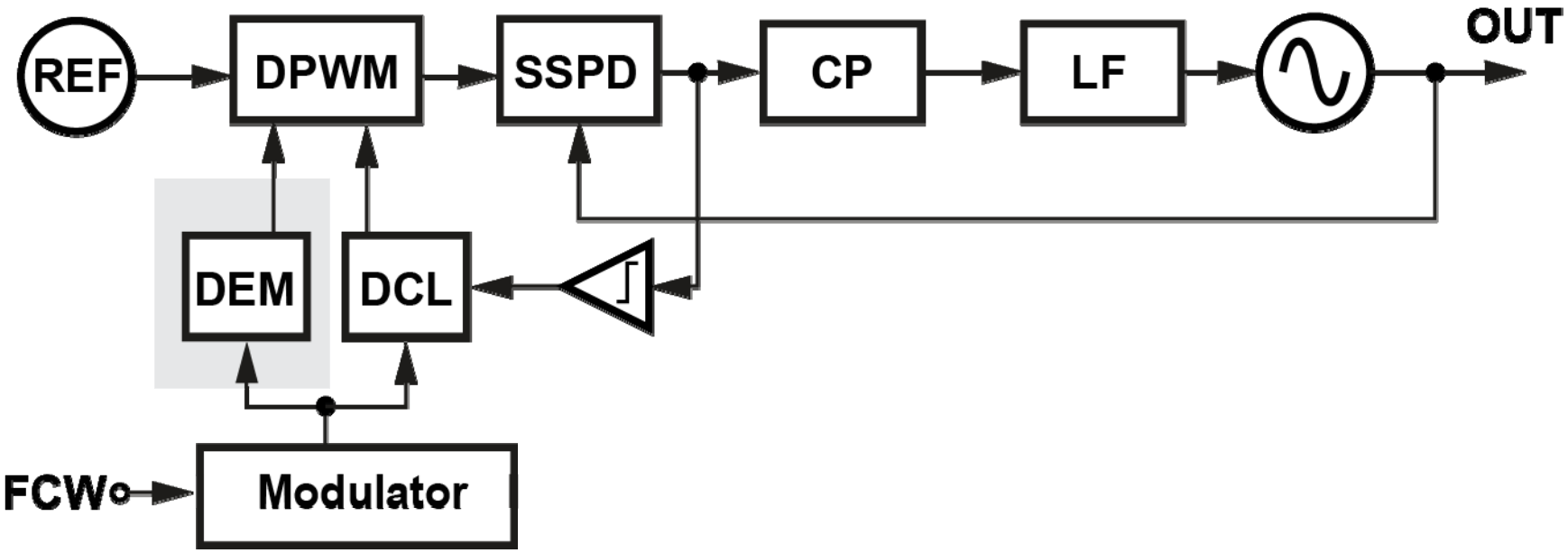


Digital Correlation Loop

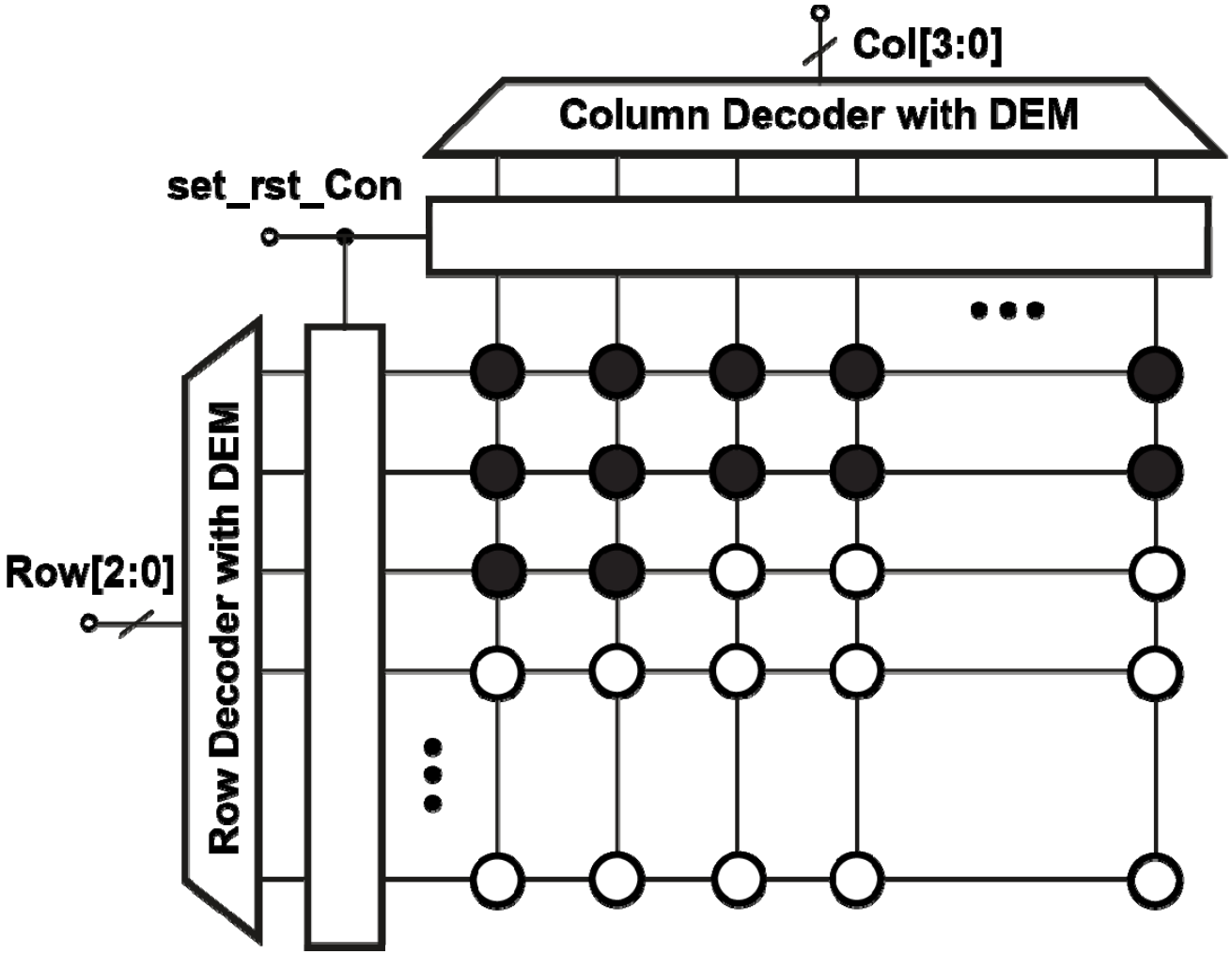


How to resolve the mismatch of the DPWM?

Proposed Architecture

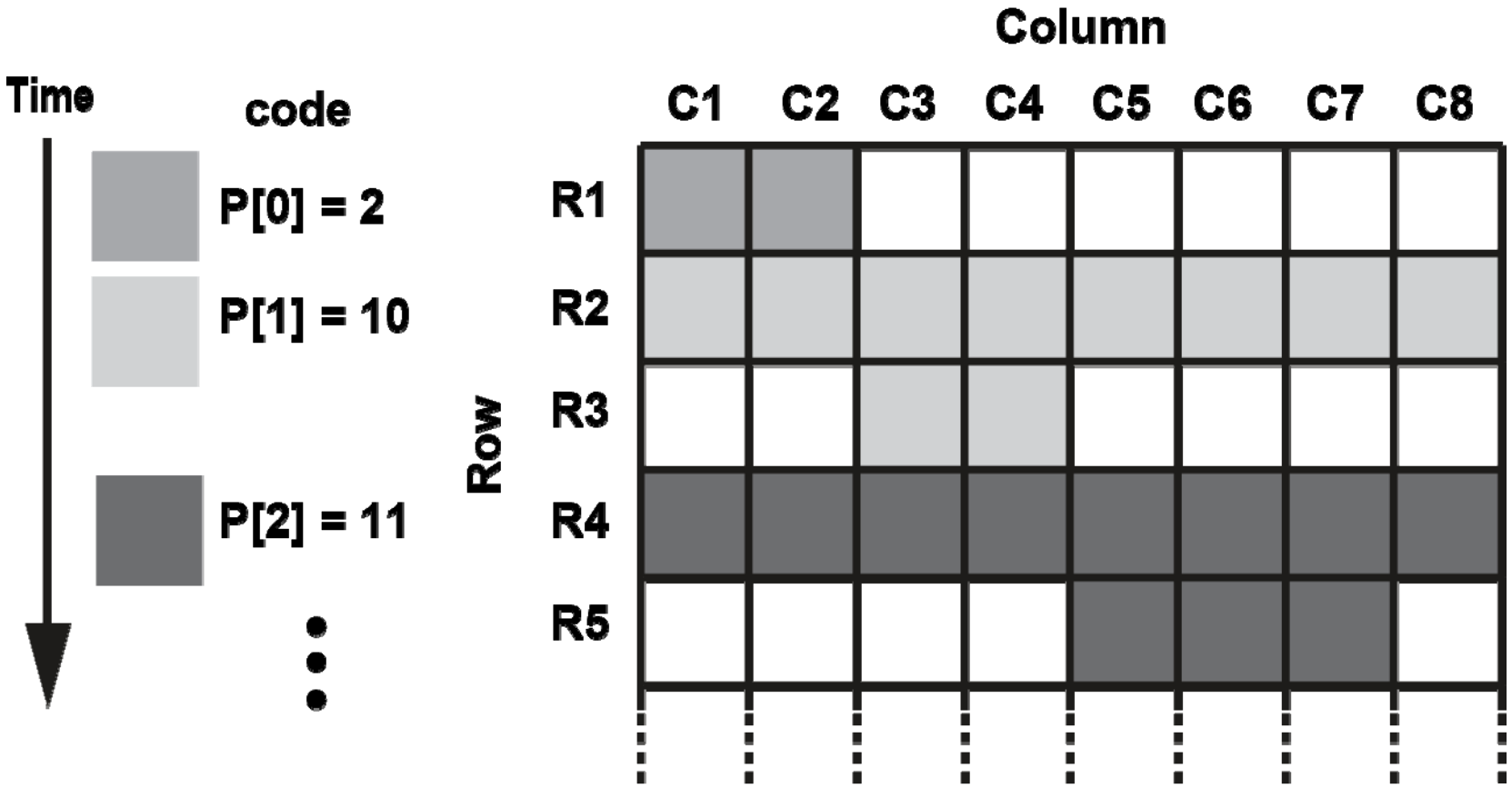


DPWM Cap Array



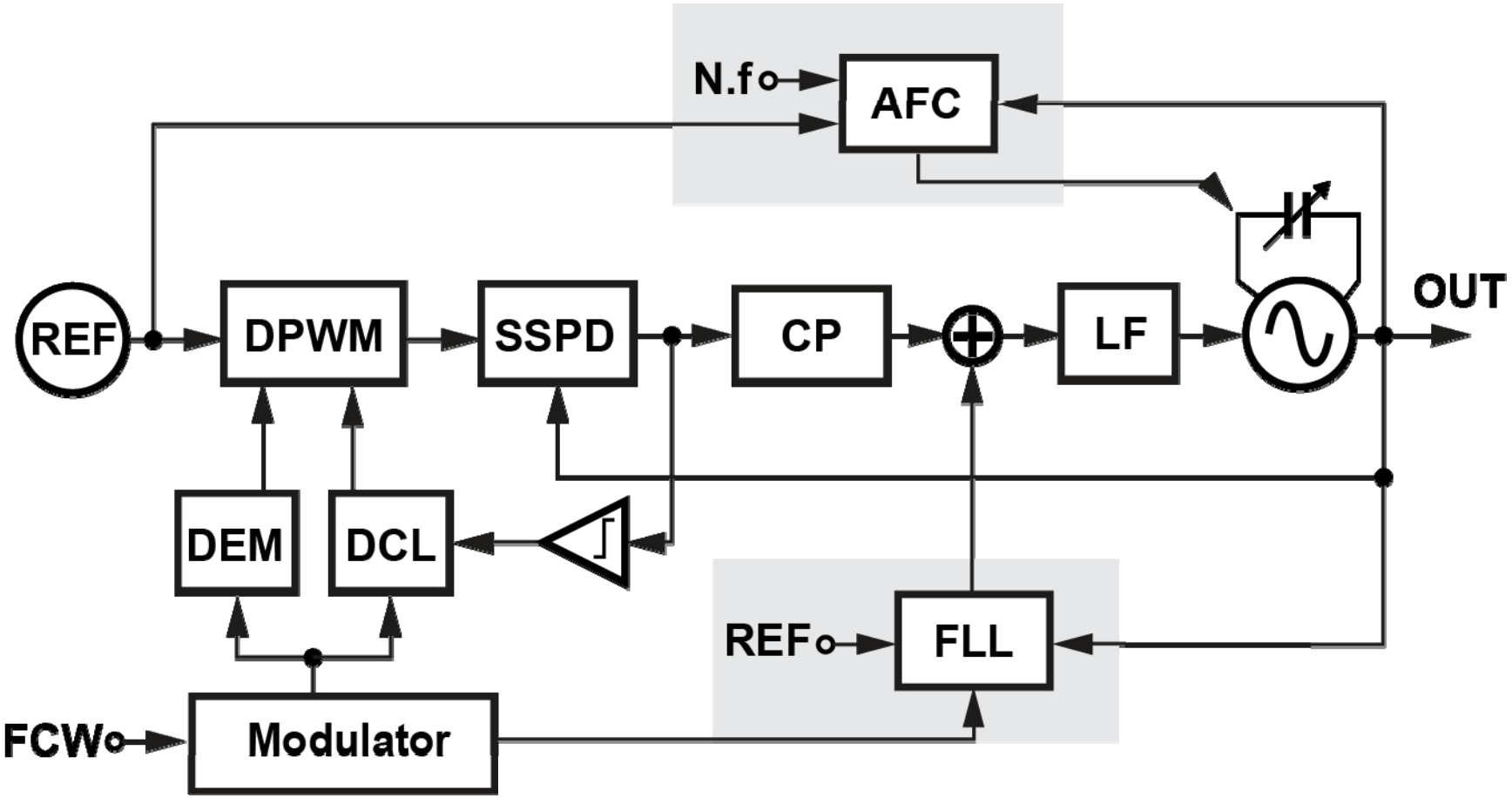
- 7-b MSB cap array and 2-b LSB caps
- 2-dimensional DEM

2-Dimensional DEM

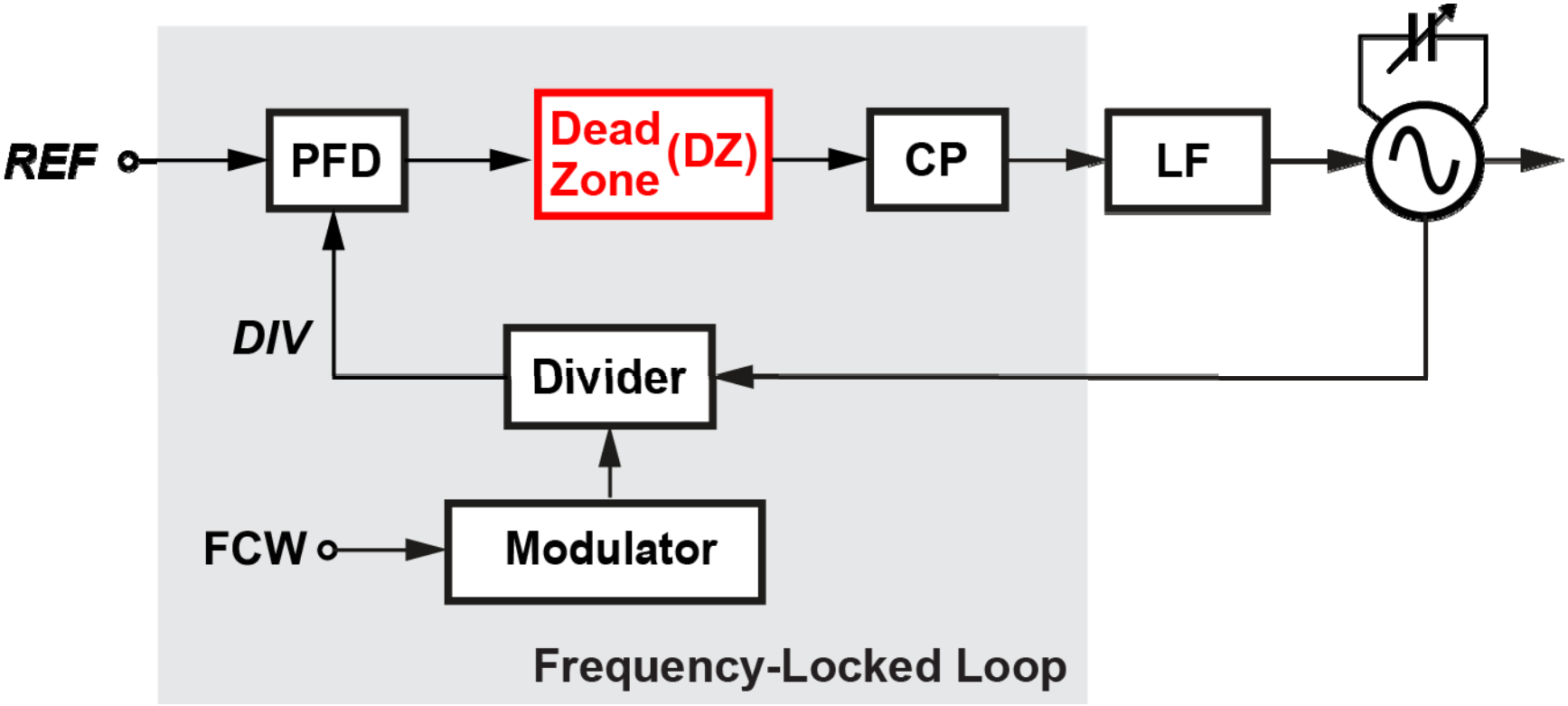


Frequency-locked aiding circuit

Proposed Architecture



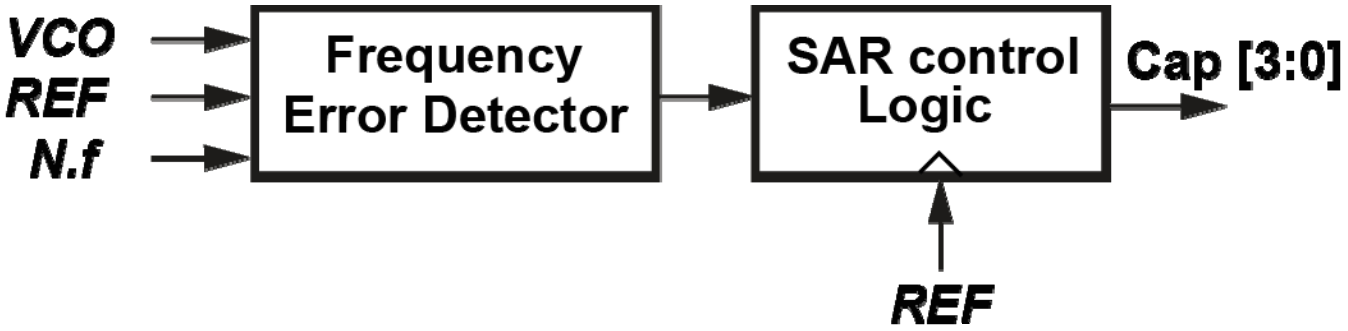
Frequency-Locked Loop

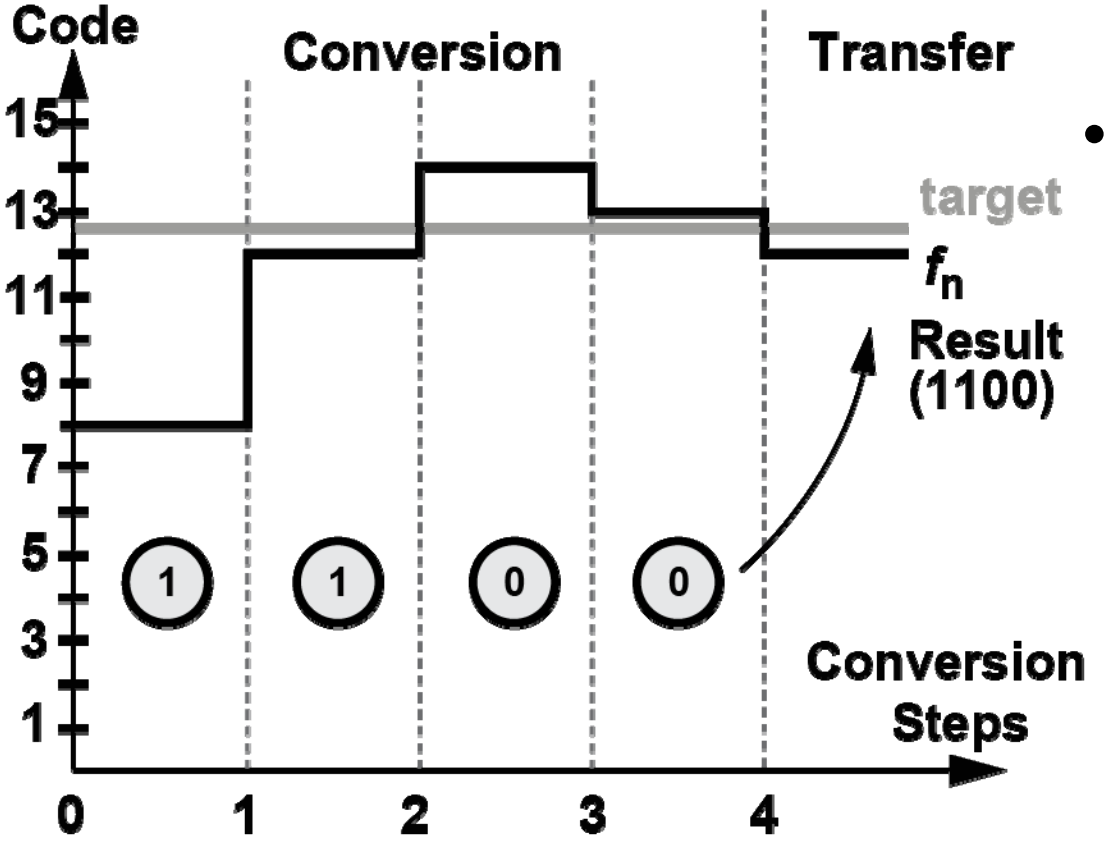


[Gao, ISSCC 09]

- **Because the SSPD has a limited locking range, a FLL is added.**

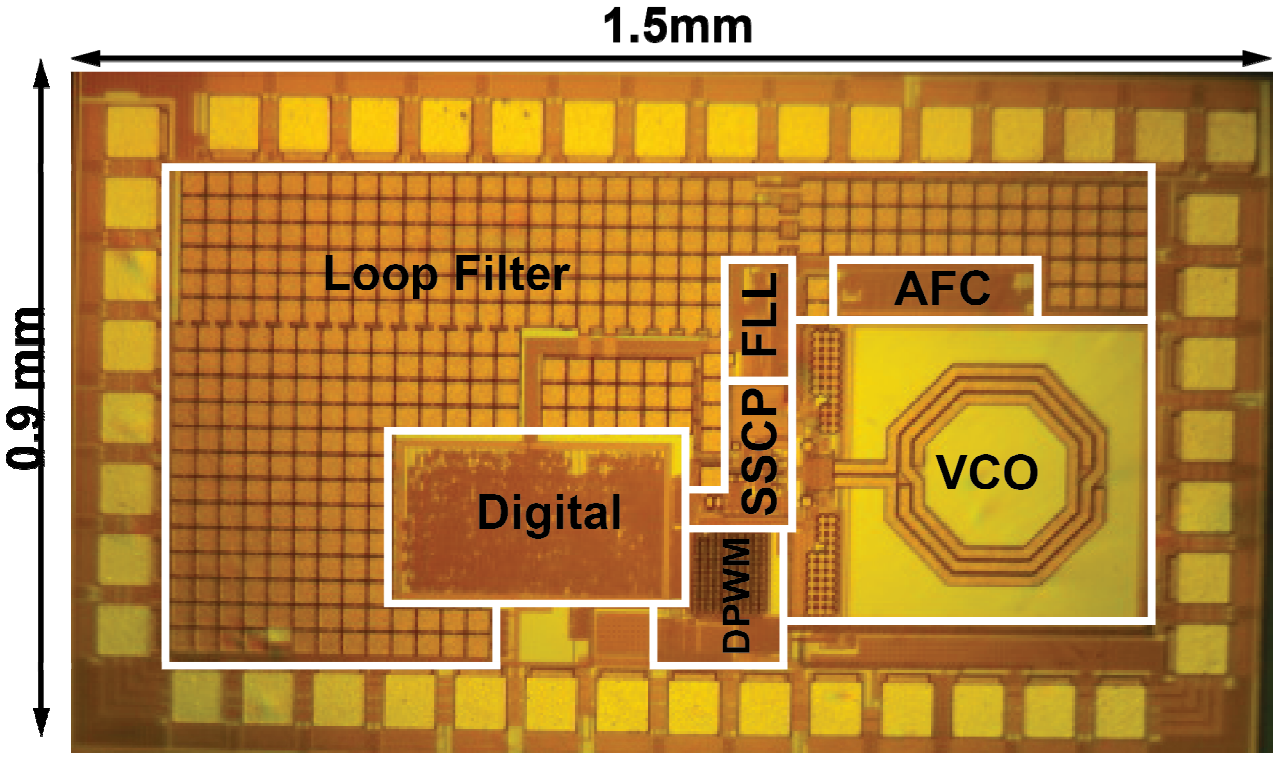
Automatic Frequency Control





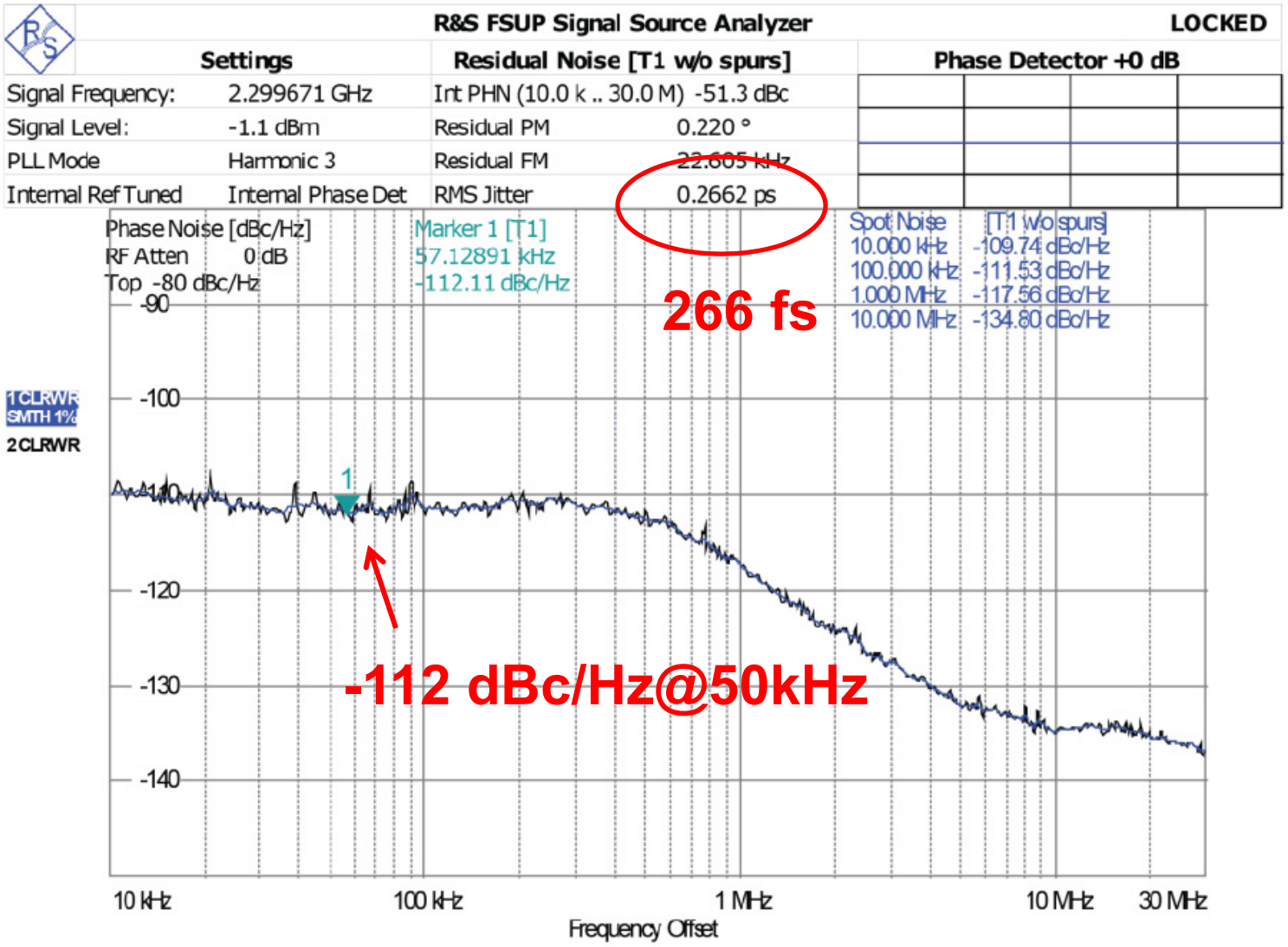
- **AFC is used to select the VCO band to extend the output frequency range.**

Die Photograph

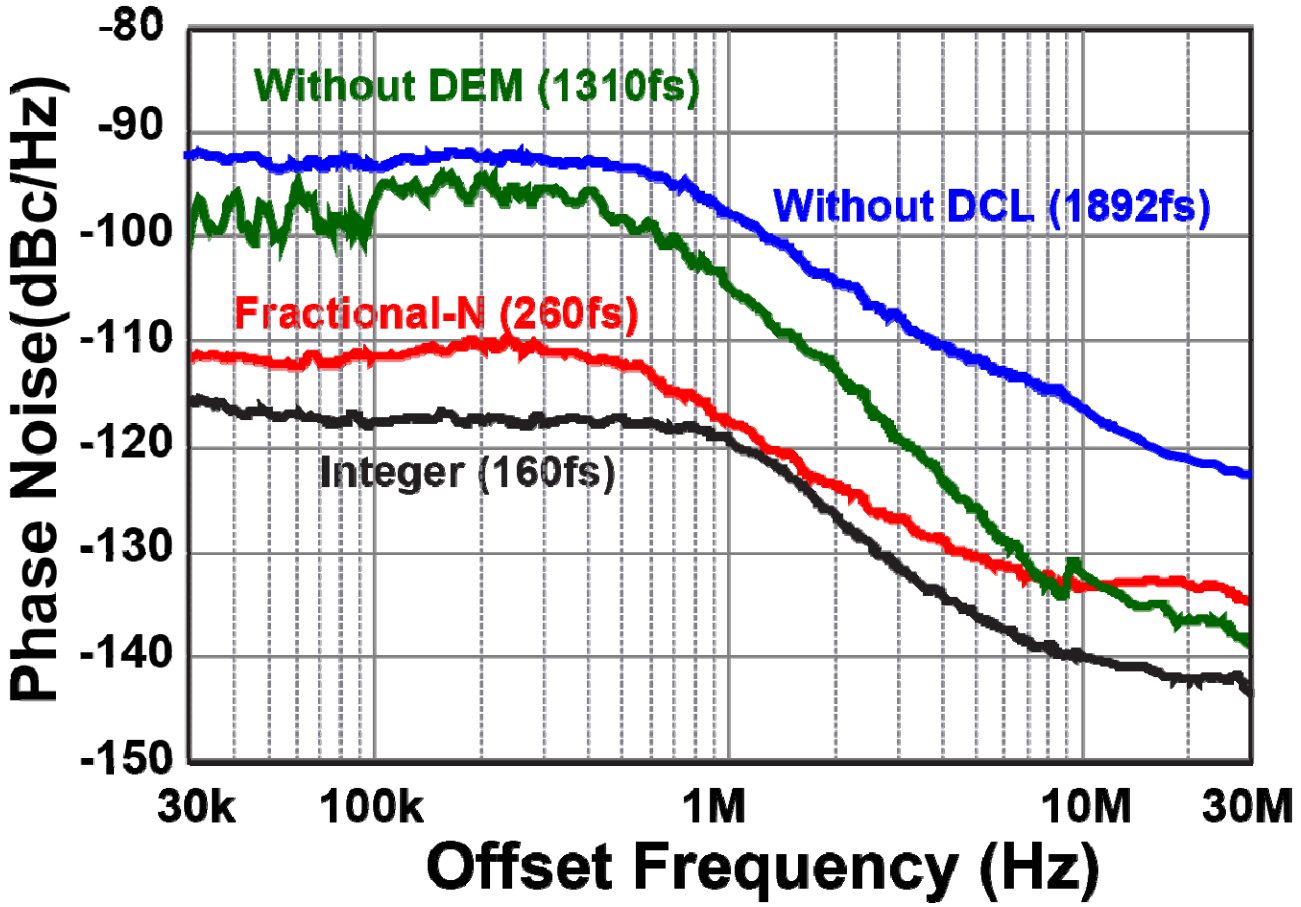


- TSMC 0.18 µm CMOS technology
- Core area: 1.2 x 0.6 mm^2
- Supply voltage: 1.8 V
- Power: 9.6 mA

Measured Phase Noise

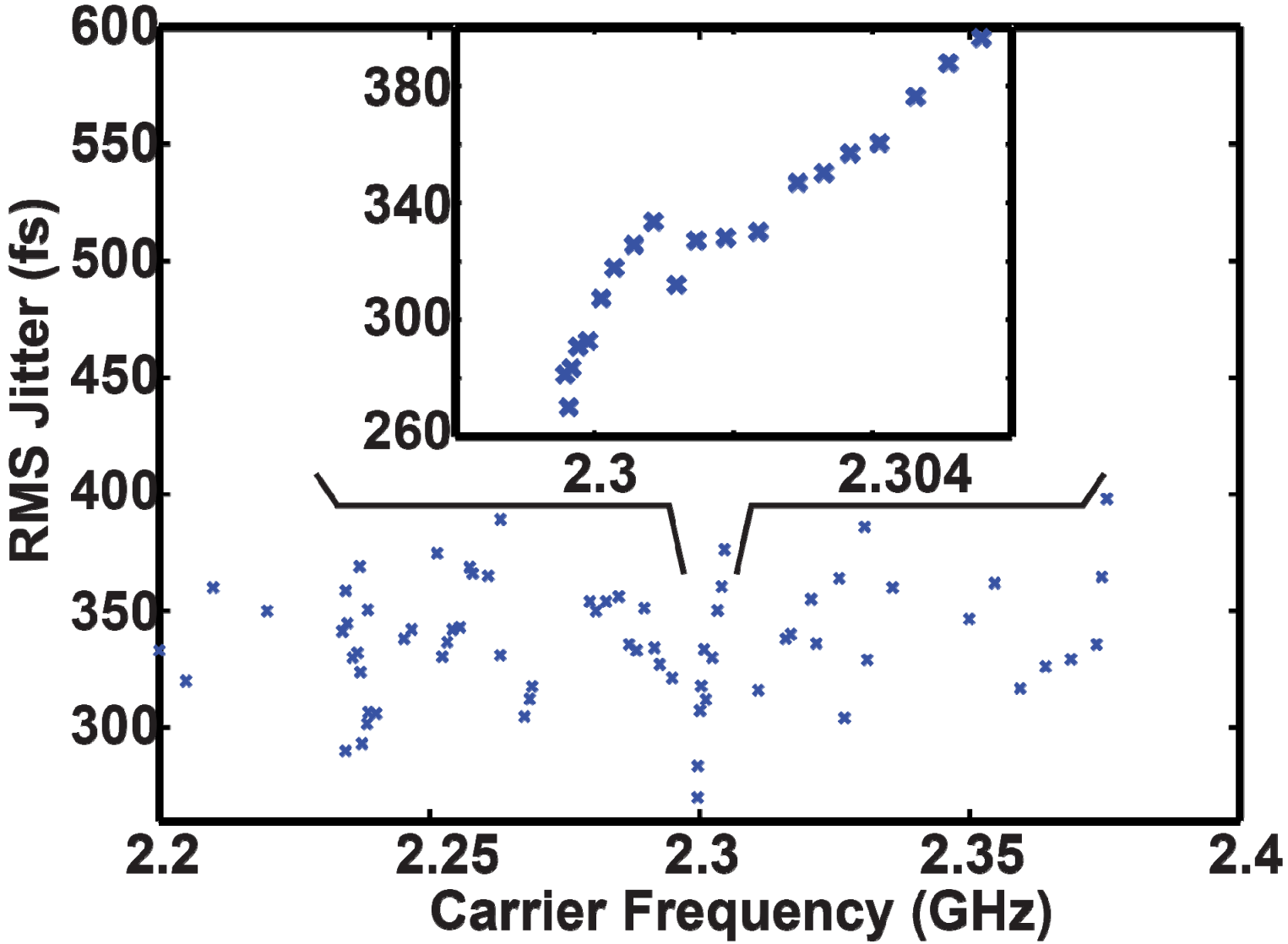


Measured Phase Noise

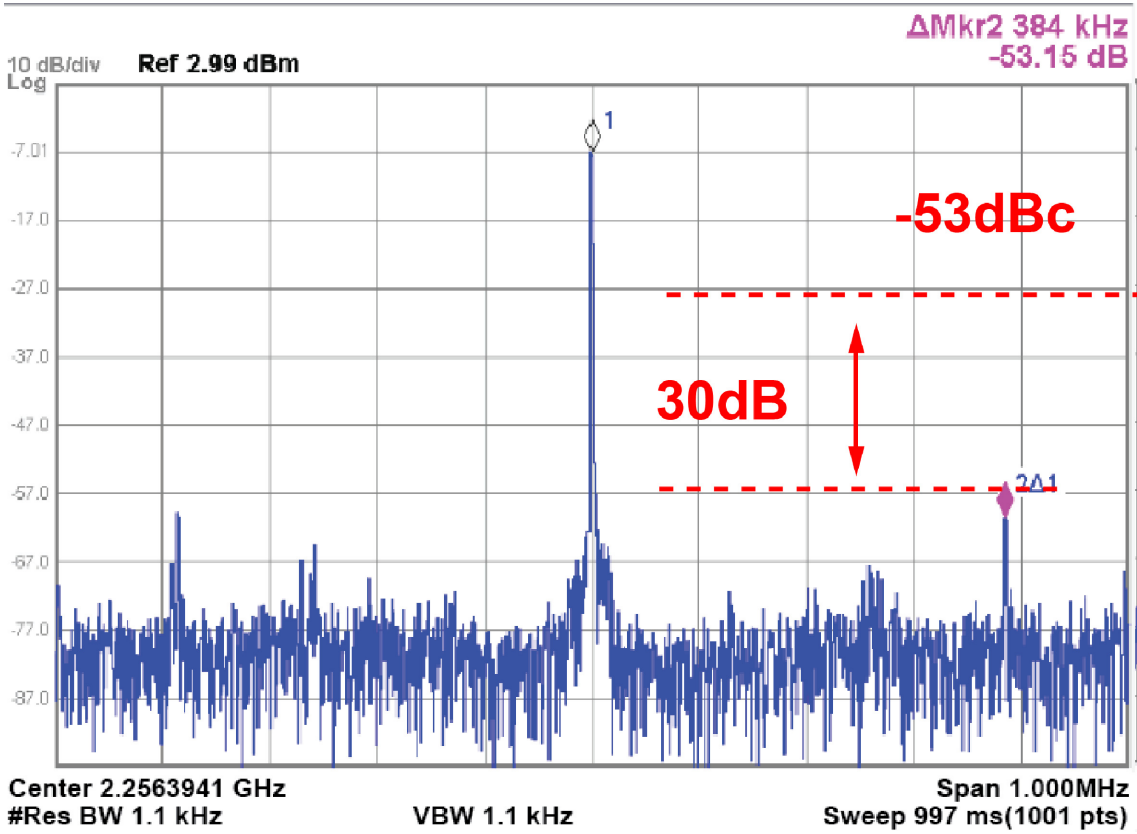


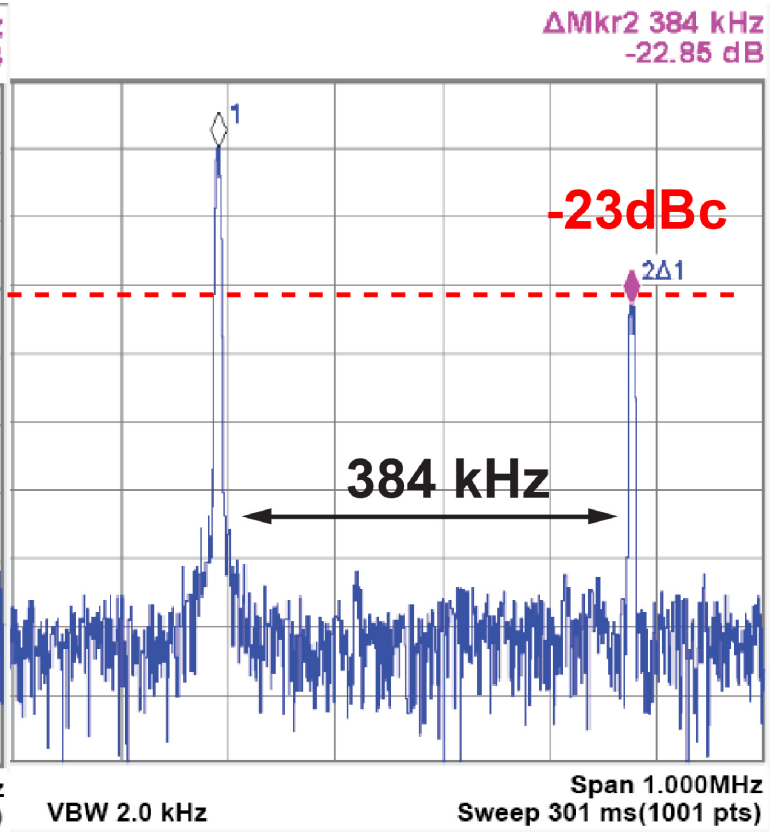
- Integrated rms jitter [integer]: 160 fs
- Integrated rms jitter [fractional-N]: 260 fs

Measured Jitter vs. Channels



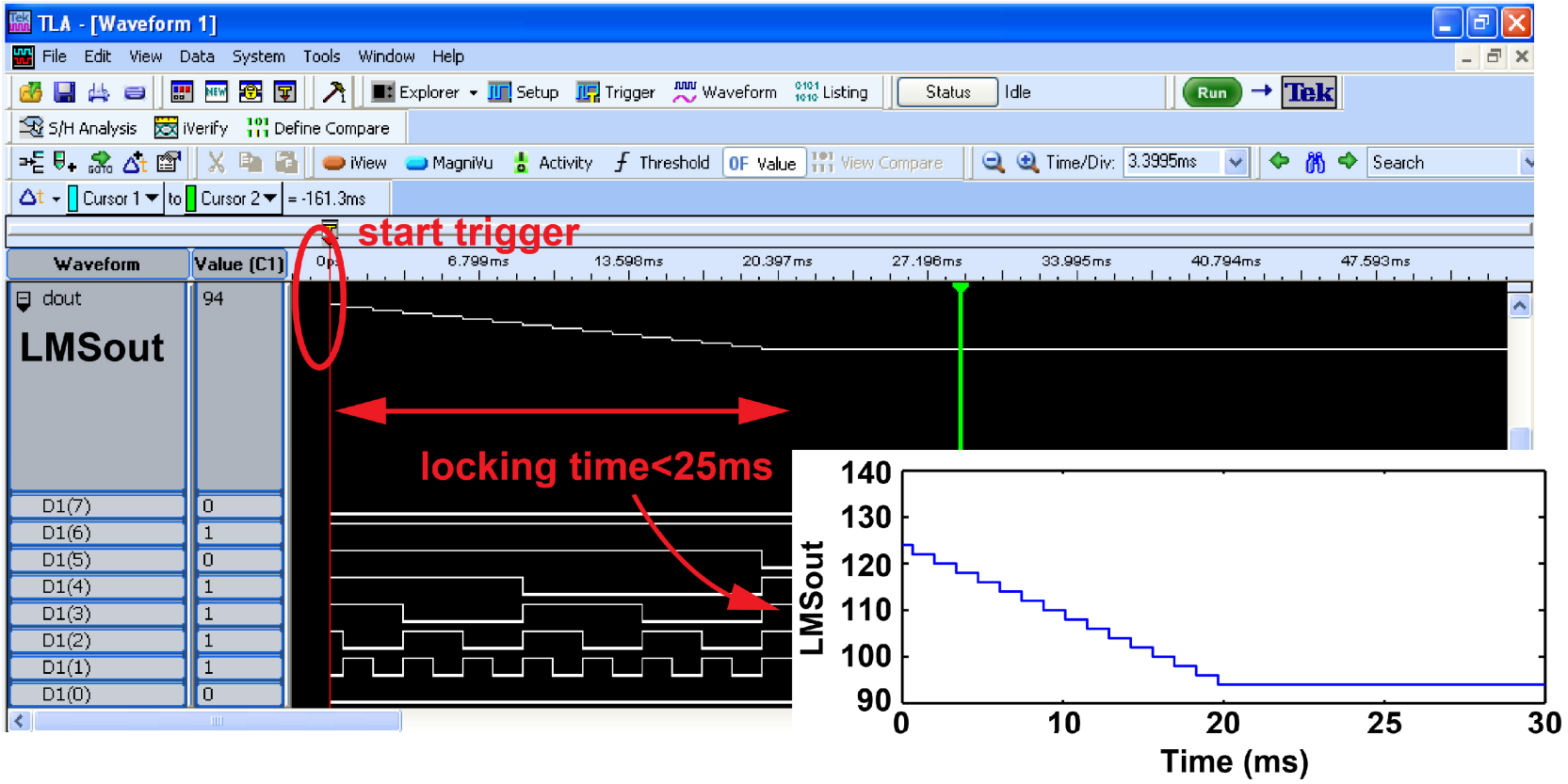
Measured Fractional Spur





- **By activation DEM and DCL, fractional spur can be reduced from -23 dBc to -53 dBc.**

Measured Convergence of DCL

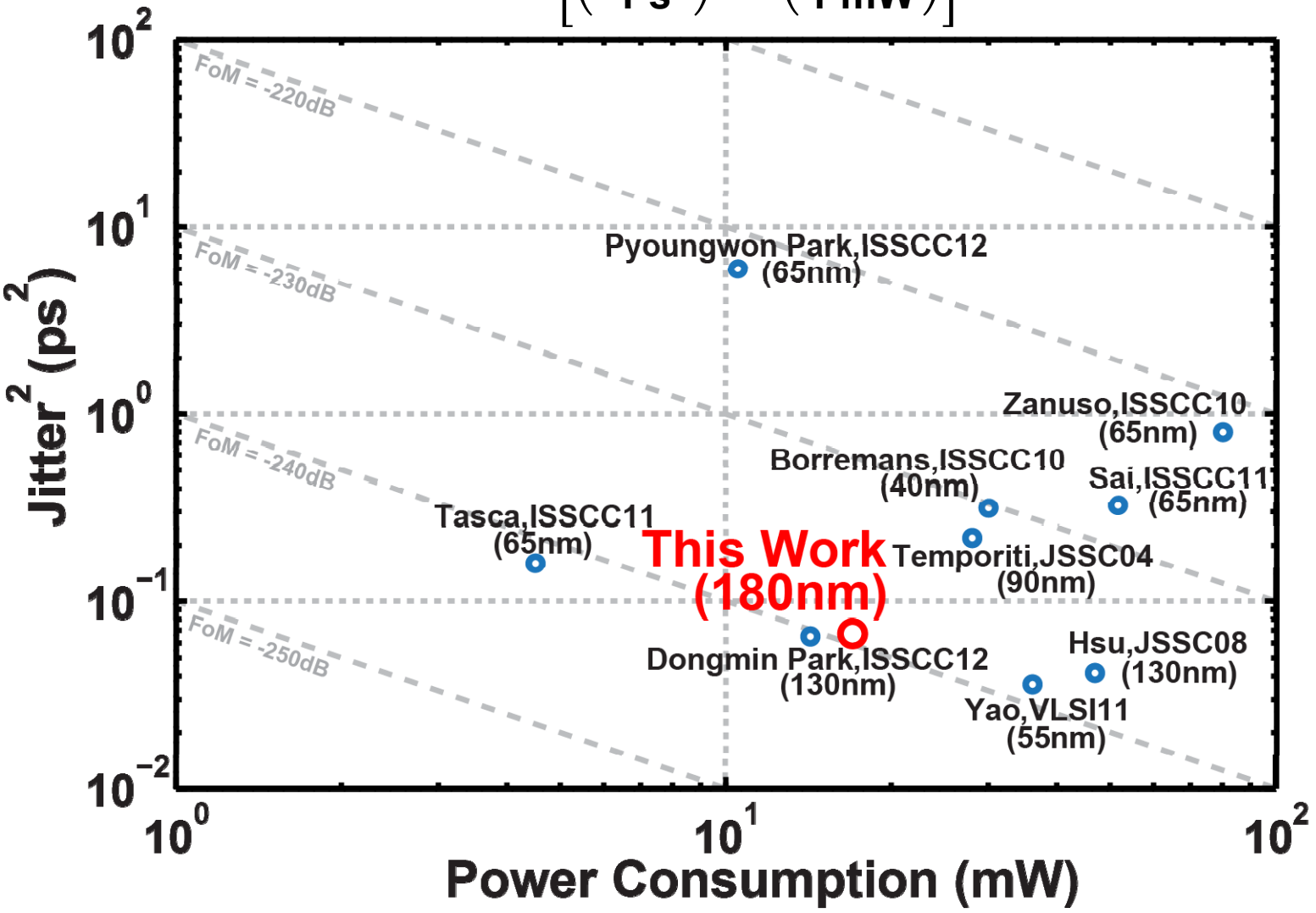


Performance Summary

	ISSCC 08	ISSCC 11	ISSCC 12	This Work
Architecture	Digital	Digital	Analog	Analog
Output (GHz)	3.62~3.67	2.9~4	0.57~0.6	2.12~2.4
In-band Noise (dBc/Hz)	-108 @400kHz	-102 @50kHz	N/A	-112 @50kHz
Integrated Jitter (ps)	0.20~0.30 (1k~40M)	0.40~0.56 (3k~30M)	2.45~4.23 (100~40M)	0.26~0.40 (10k~30M)
Ref. Spur (dBc)	-65	-72	N/A	-55
Frac. Spur (dBc)	-42	-42	N/A	-53
Power (mW)	46.7	4.5	10.5	17.3
Process (nm)	130	65	65	180

Figure-of-Merit

$$\text{FoM} = 10\times\left[\left(\frac{\text{Jitter}}{1\text{ s}}\right)^2\times\left(\frac{\text{Power}}{1\text{ mW}}\right)\right]$$



Conclusions

SSPLL architecture

- **20logN lower the CP noise**
- **Eliminate the divider noise**

DPWM

- **Perform divider-less fractional-N operation**

DCL

- **Reduce the gain error**

2D-DEM

- **Reduce the random mismatch**

It achieves a low in-band noise of -112 dBc/Hz.

Acknowledgement

The authors wish to thank

- **NTU-MediaTek Lab / National Science Council (NSC) for supporting this research**
- **Chip Implementation Center (CIC) / Holtek Semiconductor for chip fabrication**

A 2GHz 130mW Direct-Digital Frequency Synthesizer with a Nonlinear DAC in 55nm CMOS

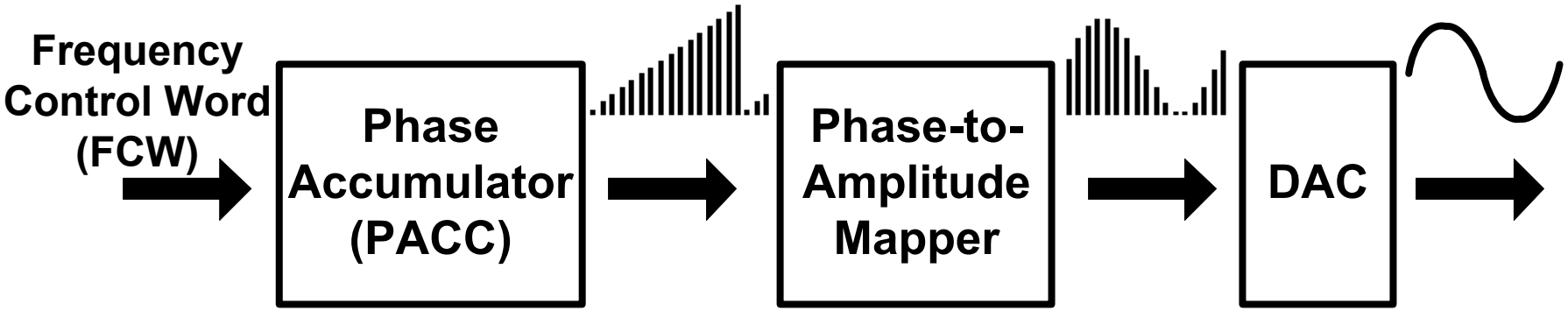
Taegeun Yoo[1], Yun-Hwan Jung[1], Hong Chang Yeoh[1,2], Yong Sin Kim[1], Sung-Mo Kang[3], Kwang-Hyun Baek[1]

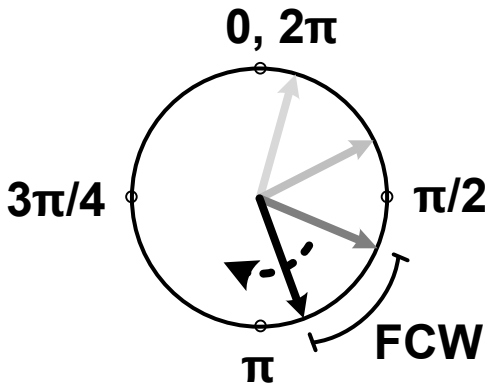
[1]Chung-Ang University, Seoul, Korea
[2]Analog Devices, San Jose, CA
[3]KAIST, Daejeon, Korea

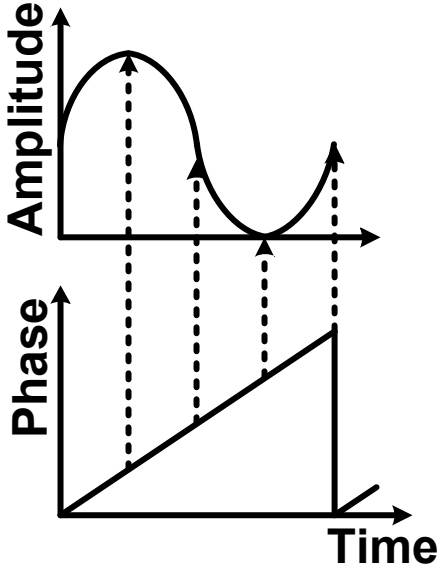
Outline

- Introduction of Direct Digital Frequency Synthesizer (DDFS)
- 3 Key Ideas
  - ► Phase accumulator with Multi-level Momentarily Activated Bias generators (M^2AB) for low power consumption
  - ► Coarse phase-based Consecutive Fine Amplitude Grouping (C^2FAG) for low decoder complexity (area)
  - ► Mixed-wave Conversion Topology (MCT) for higher spectral purity
- Measurement Results & Comparisons
- Conclusion

General concept of DDFS





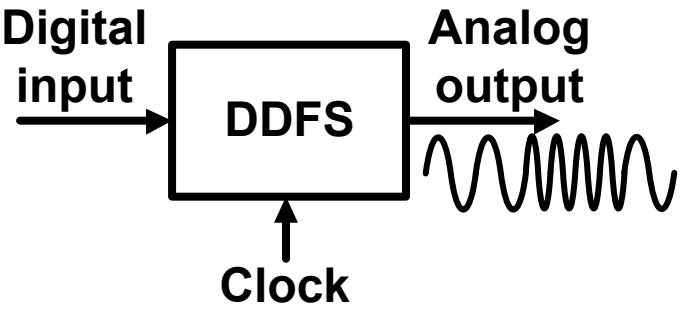


$$F_{out} = \frac{F_{clk} \cdot FCW}{2^N}$$

F_{clk} : Clock Freq.
N : FCW width

Characteristics of DDFS

DDFS is a data converter(DAC) based frequency synthesizer



► Advantages

- Wide tuning range
- Phase and frequency agility
- Fine frequency tuning resolution
- Minimal jitter addition

► Disadvantages

- High power consumption
- Large area
- Spectral purity limitation

Direct Digital Frequency Synthesizers

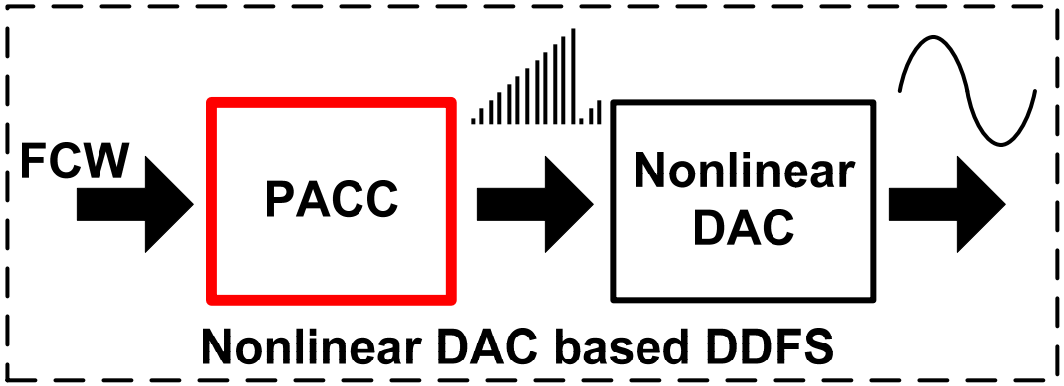
Digital Mapping
- High power
- Large area
- High accuracy

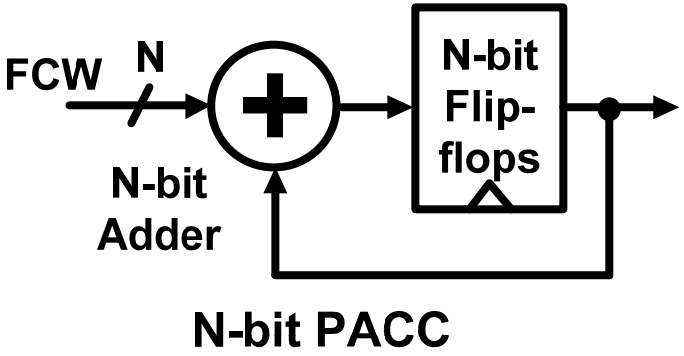
Analog Mapping
- Low power
- Small area
- Low accuracy

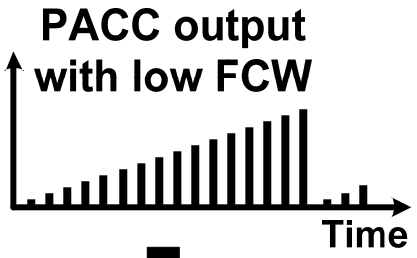
Nonlinear DAC based mapping
- Low power
- Small area
- Medium accuracy

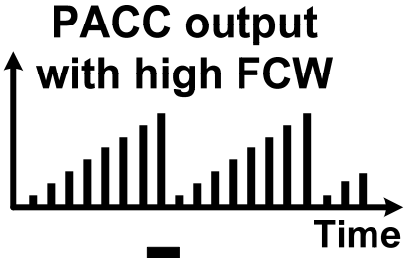
Nonlinear DAC (NLDAC) based design shows good balance between power, speed and conversion accuracy

Conventional Phase Accumulator



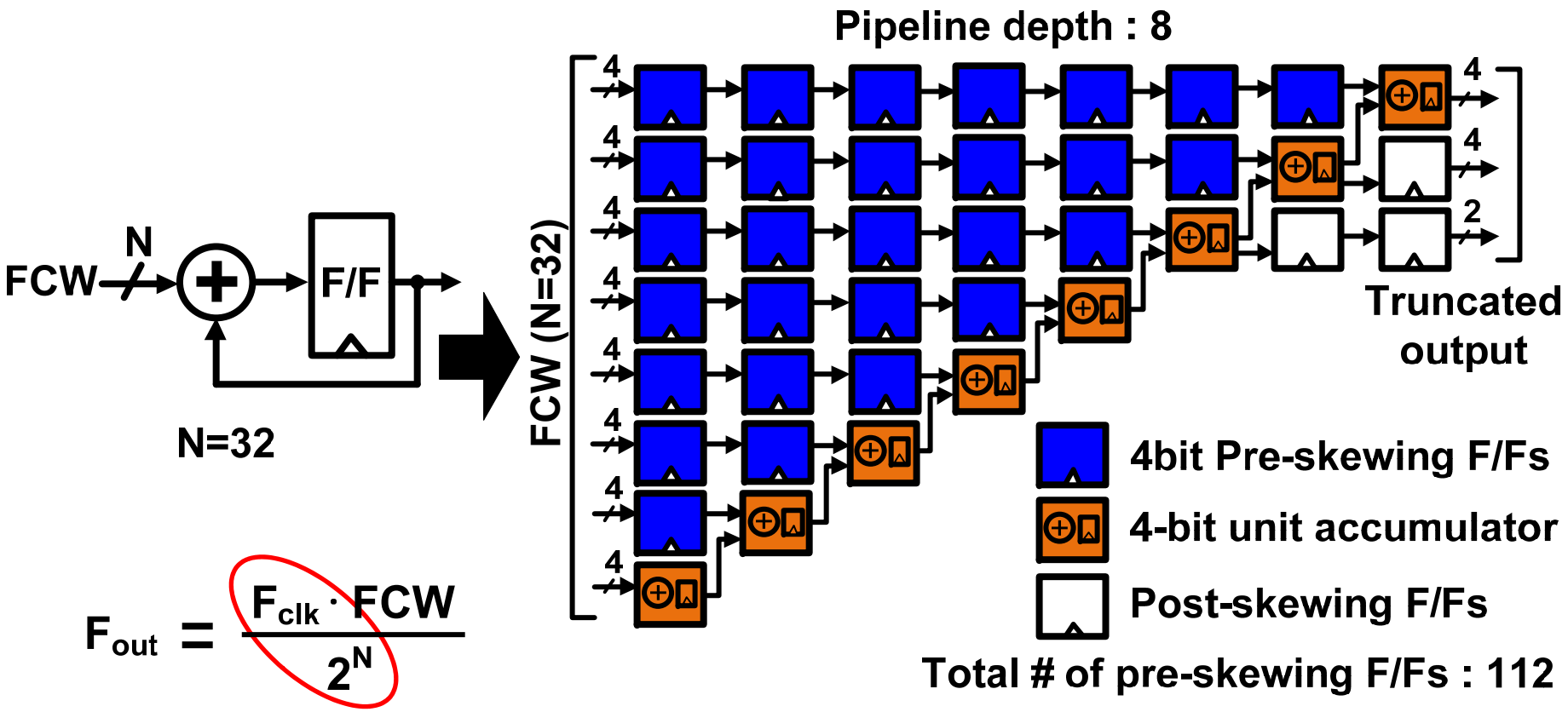






$$F_{out} = \frac{F_{clk} \cdot FCW}{2^N}$$

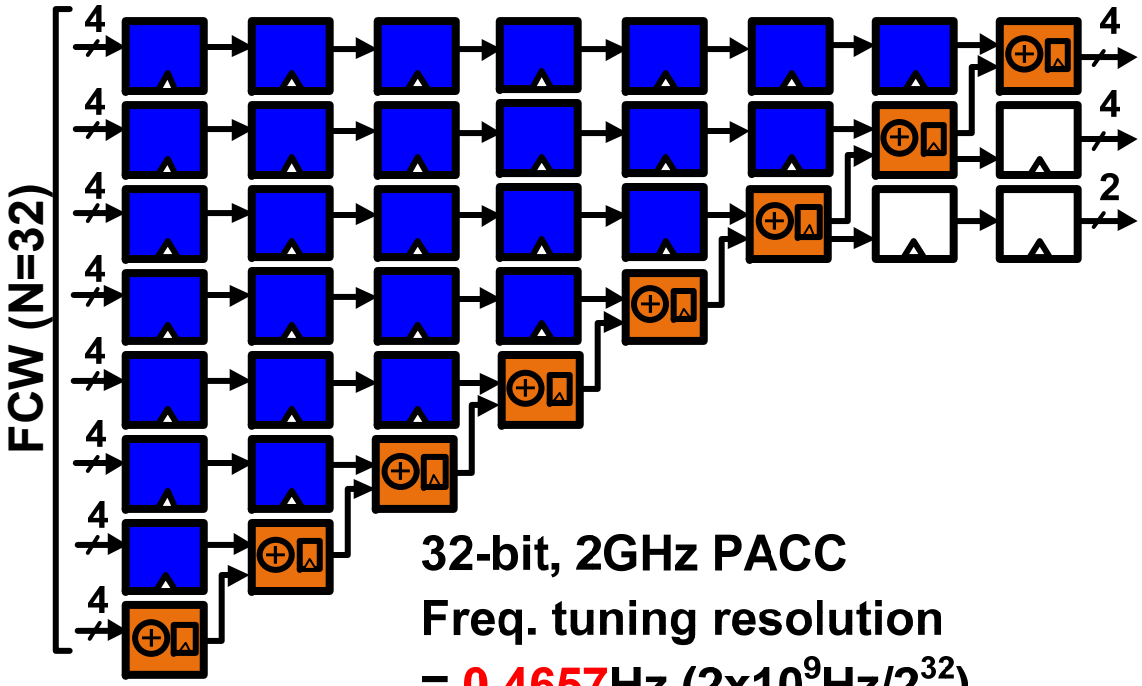
Pipelined Phase Accumulator



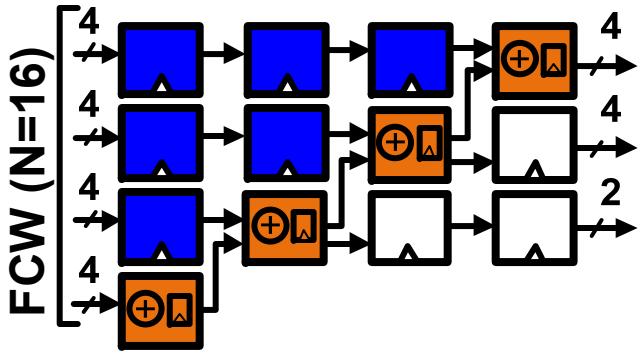
$$F_{out} = \frac{F_{clk} \cdot FCW}{2^N}$$

Pipelining requires additional power and area

Frequency tuning resolution upon N



32-bit, 2GHz PACC
Freq. tuning resolution
= 0.4657Hz ($2x10^9Hz/2^{32}$)

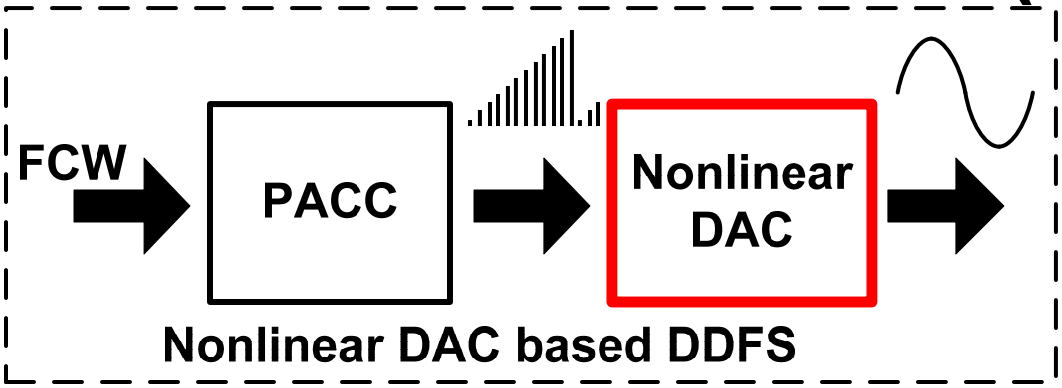


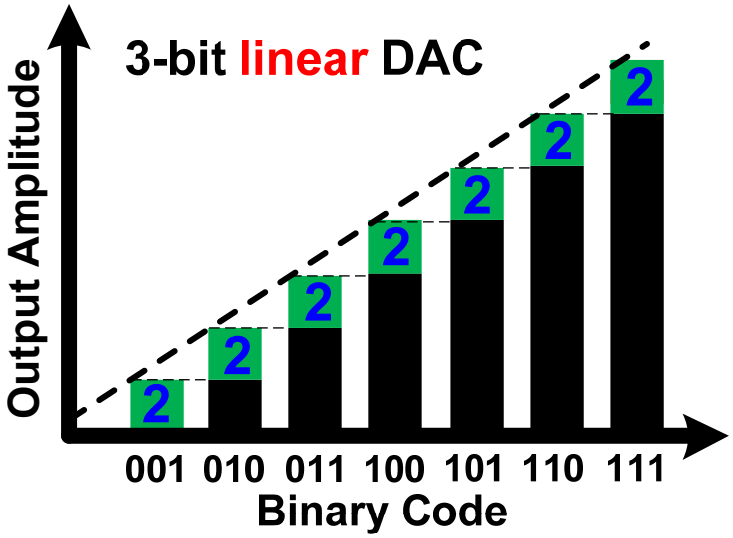
16-bit, 2GHz PACC
Freq. tuning resolution
= 30517Hz ($2x10^9Hz/2^{16}$)

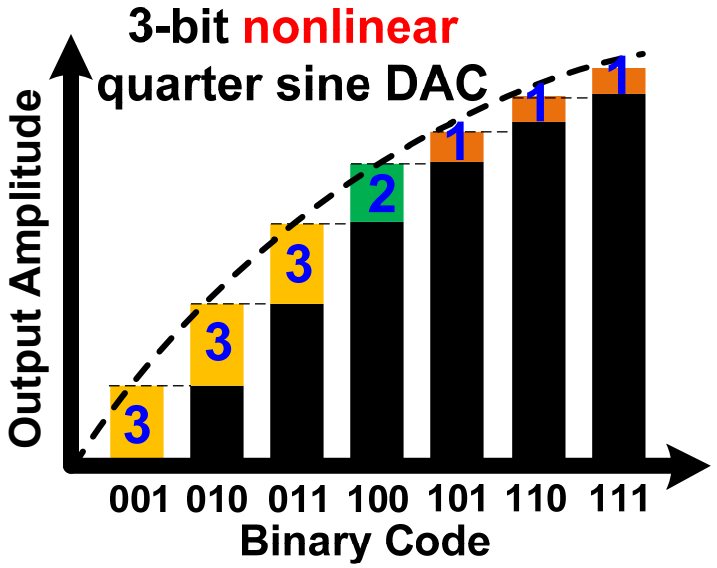
Finer frequency tuning

Rough frequency tuning

Conventional Nonlinear DAC (NLDAC)

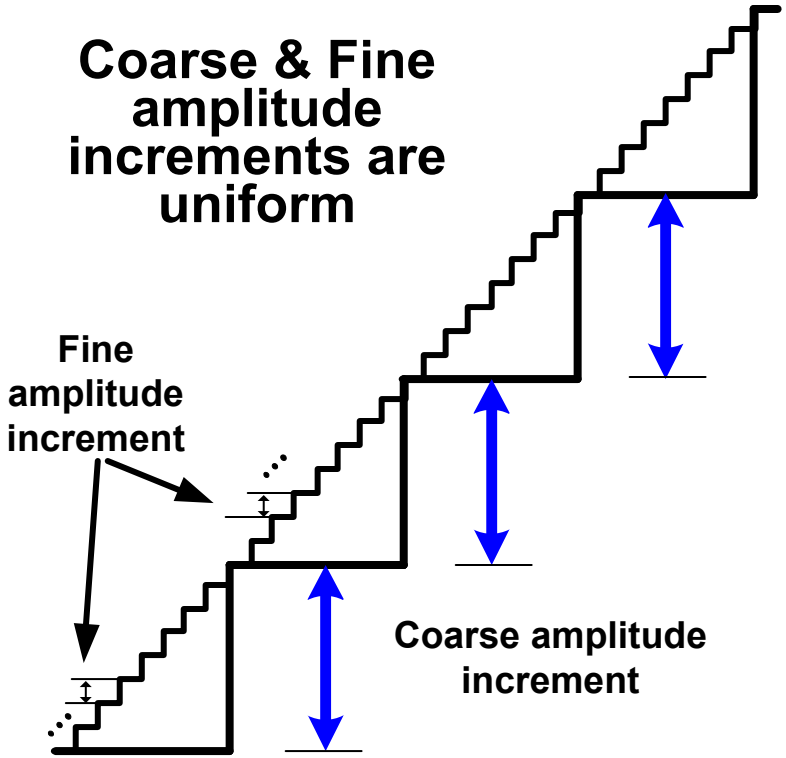




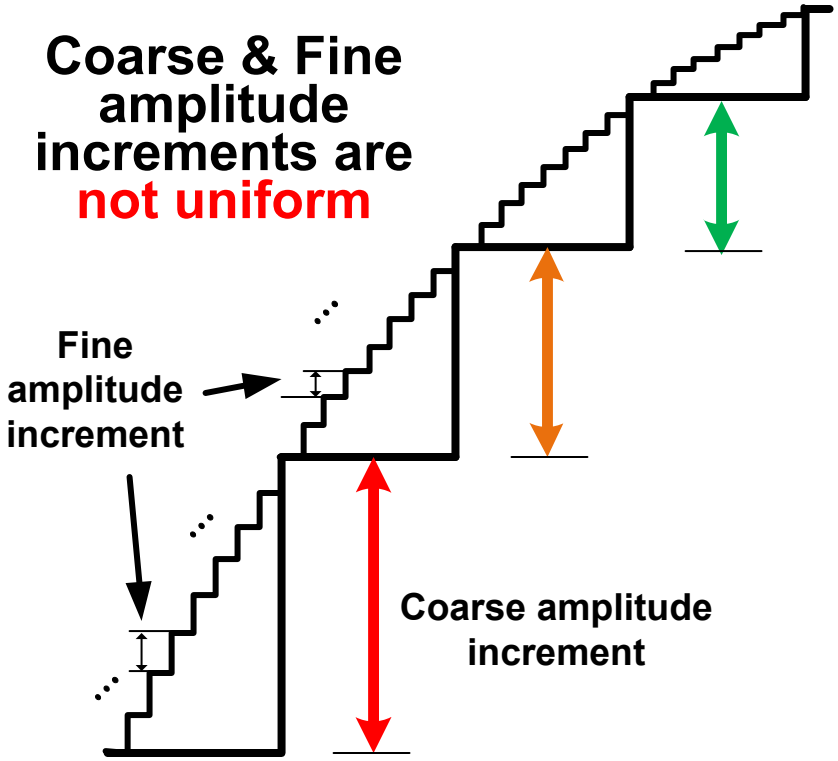


- ▶ $2^M - 1$ switches for M bits (less than 6-bit is preferred)
- ▶ Segmentation is required for higher resolution

Segmentation in DACs



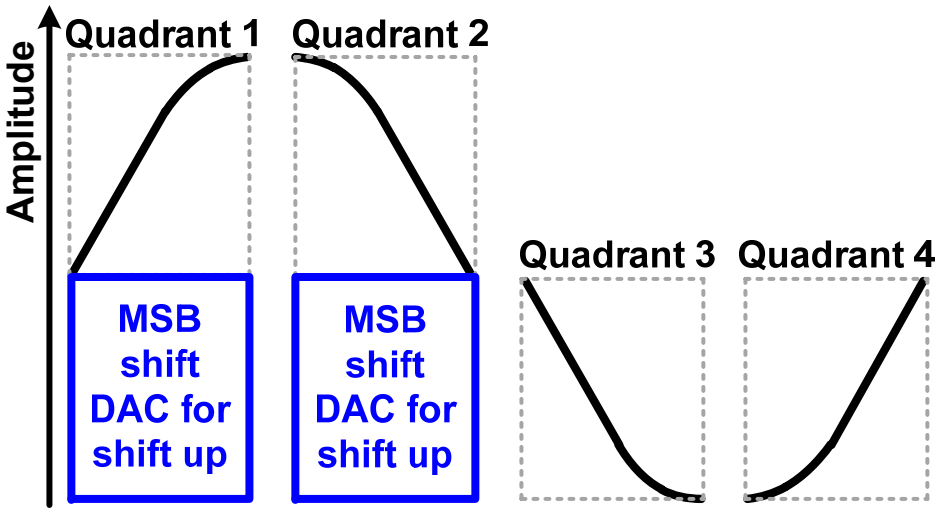
Linear DAC



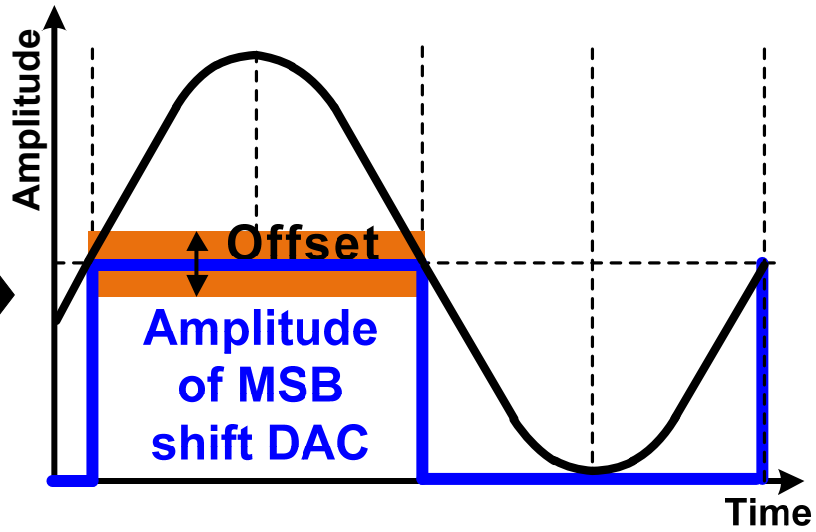
Nonlinear DAC

Nonlinear segmentation is not easily implementable

Conventional Quarter Sine-wave Technique



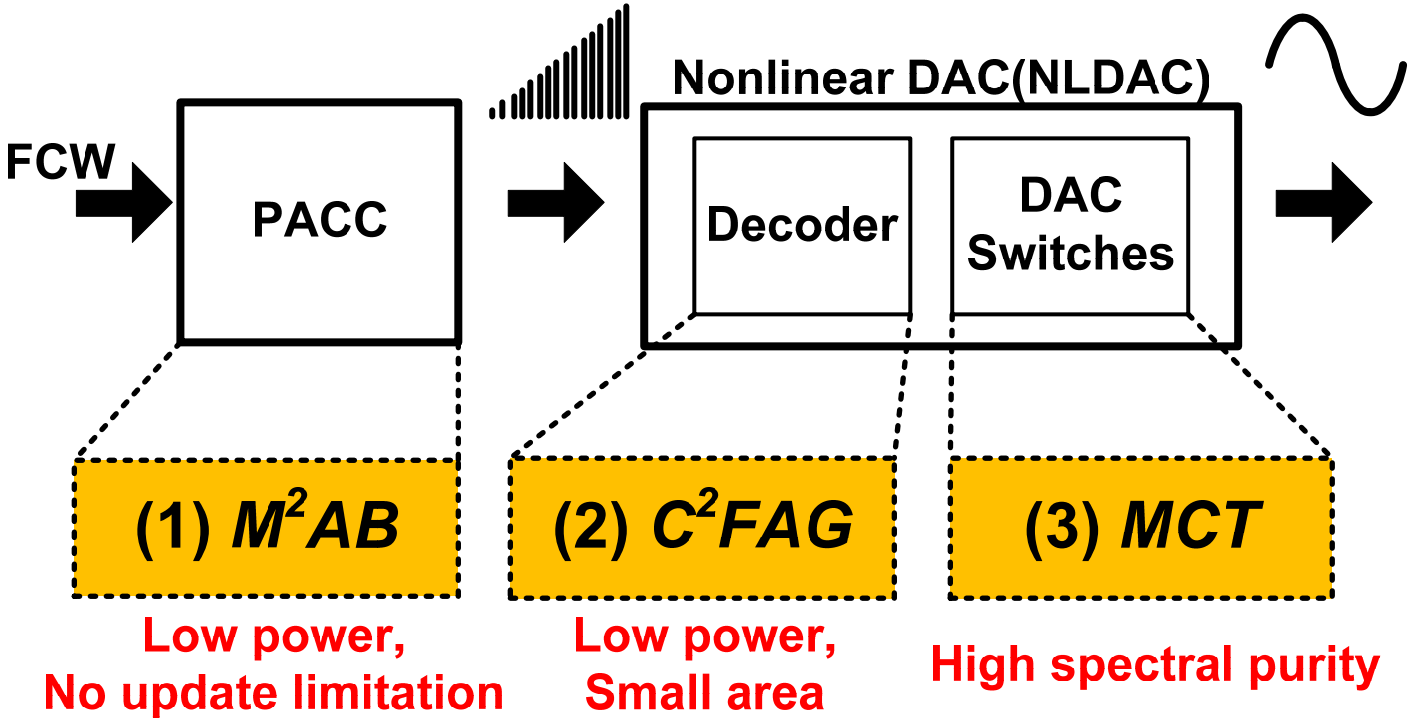
Conventional Quarter Sine-wave Technique (QST) with NLDAC



Synthesized Sine-wave

MSB shift DAC can cause the offset & harmonic distortion

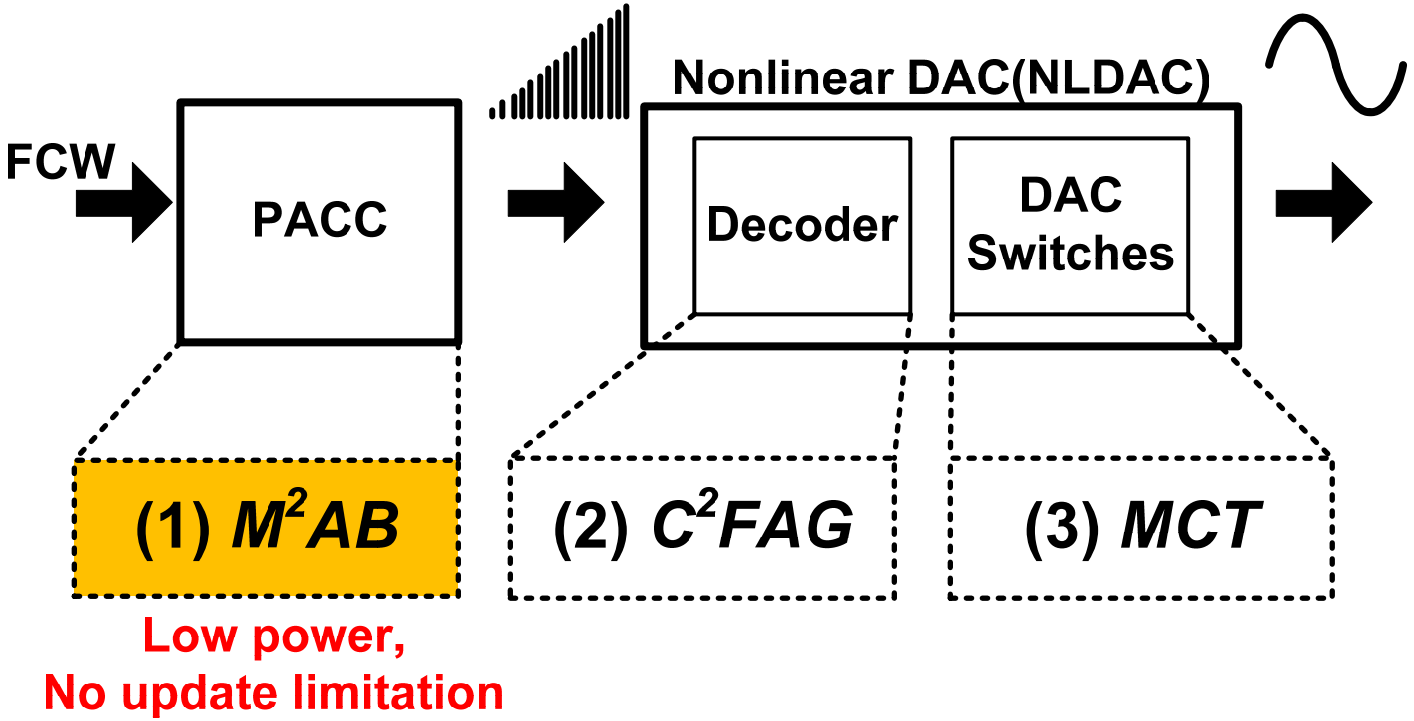
Proposed Three Techniques



(1) *M²AB* : Multi-level Momentarily Activated Bias

(2) *C²FAG* : Coarse phase-based Consecutive Fine Amplitude Grouping

(3) *MCT* : Mixed-wave Conversion Topology

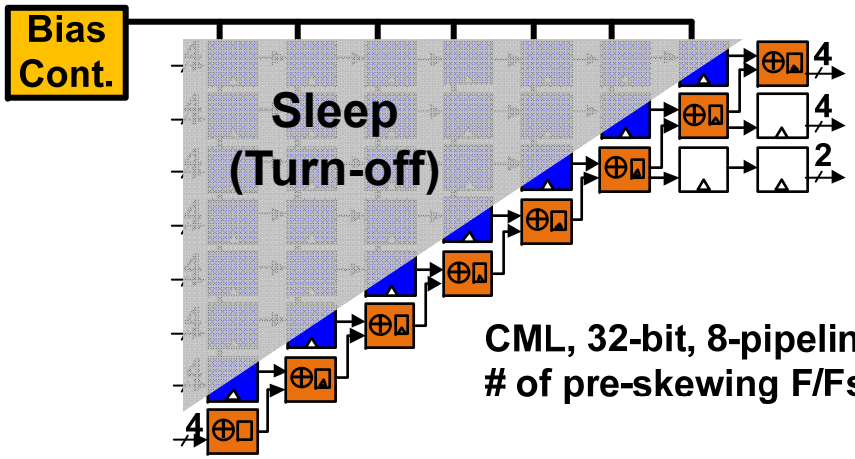


(1) *M²AB* : Multi-level Momentarily Activated Bias

(2) *C²FAG* : Coarse phase-based Consecutive Fine Amplitude Grouping

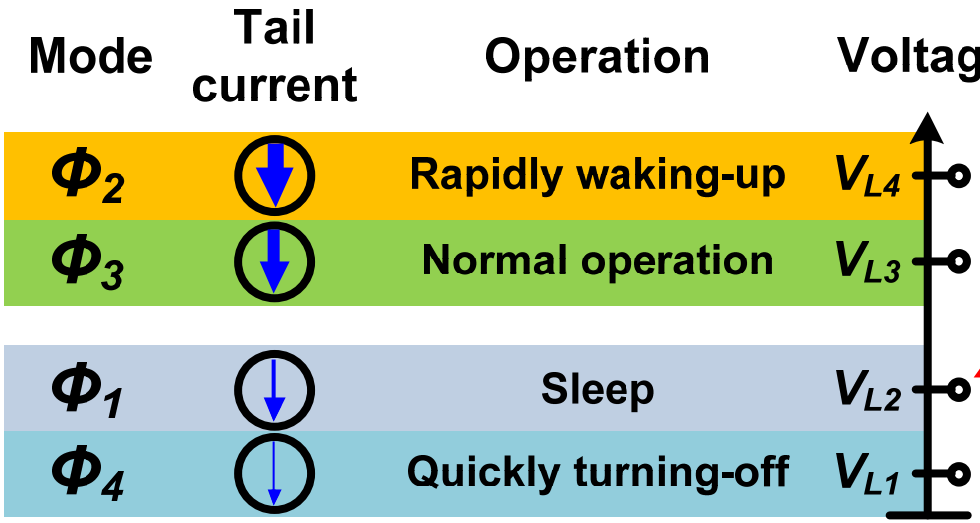
(3) *MCT* : Mixed-wave Conversion Topology

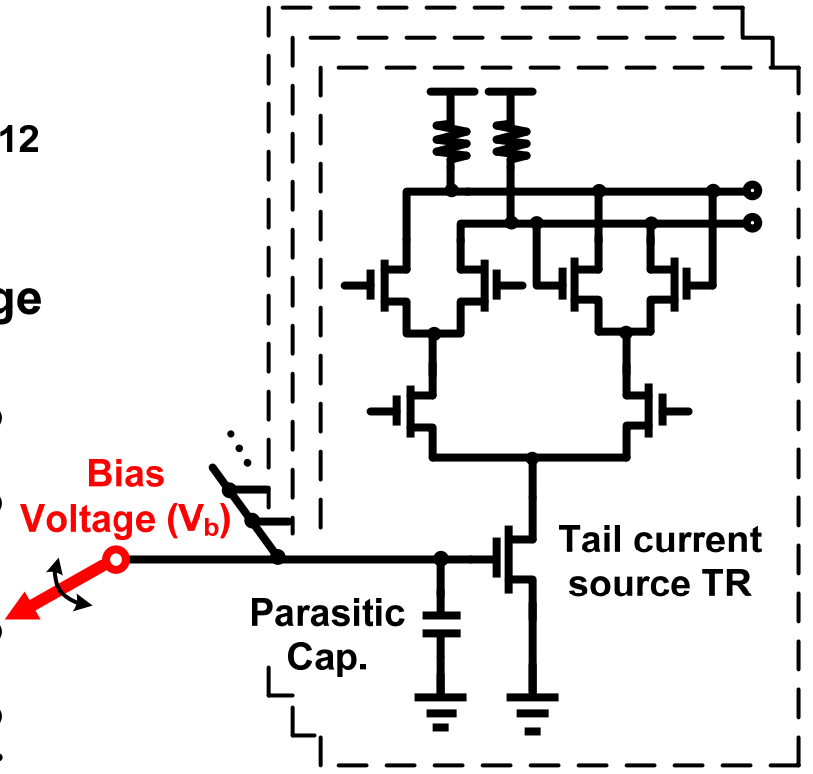
Concept of Proposed Bias Voltage Control



CML, 32-bit, 8-pipeline
# of pre-skewing F/Fs : 112

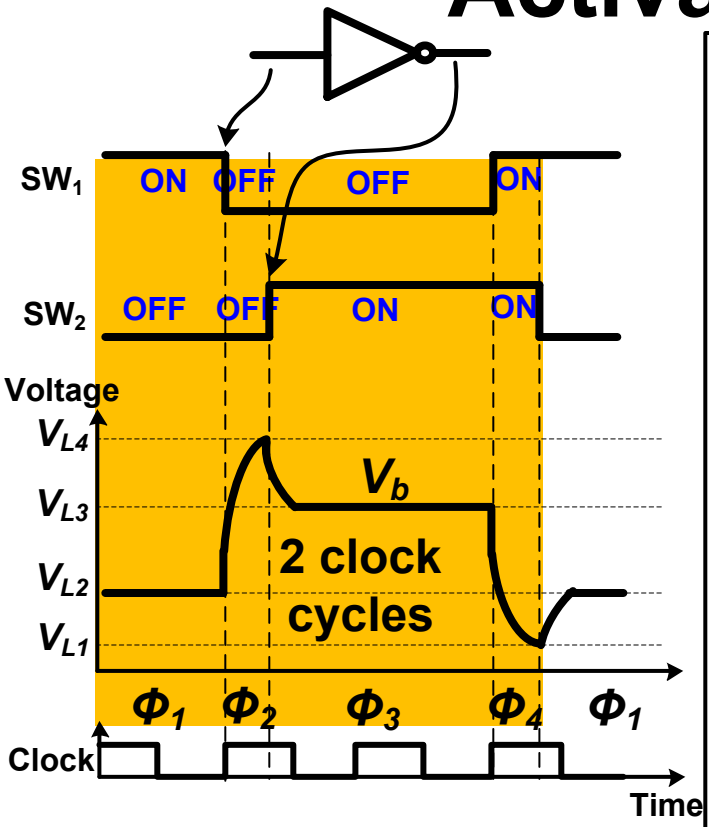
Current mode logic (CML) based latch in the pre-skewing F/Fs

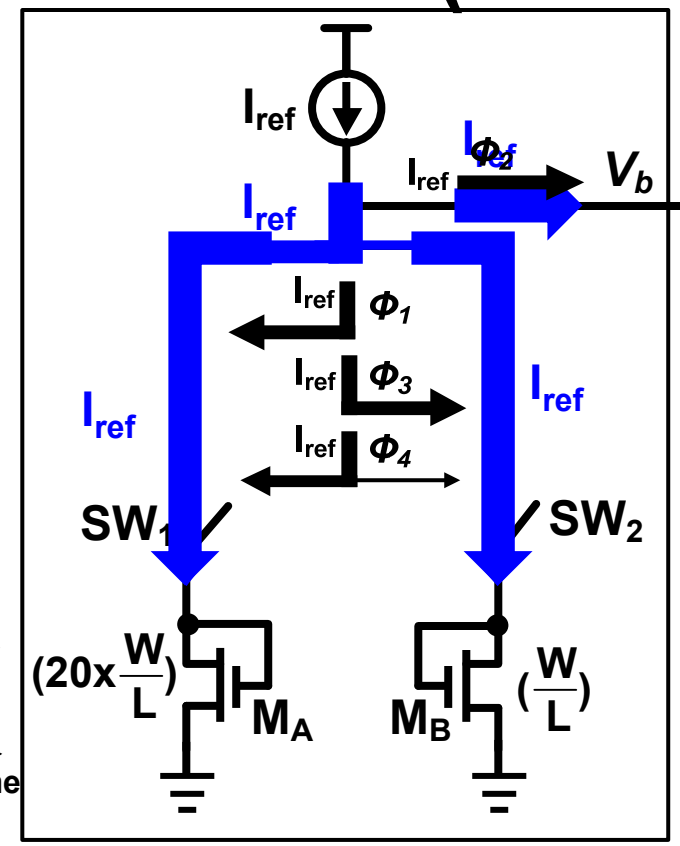


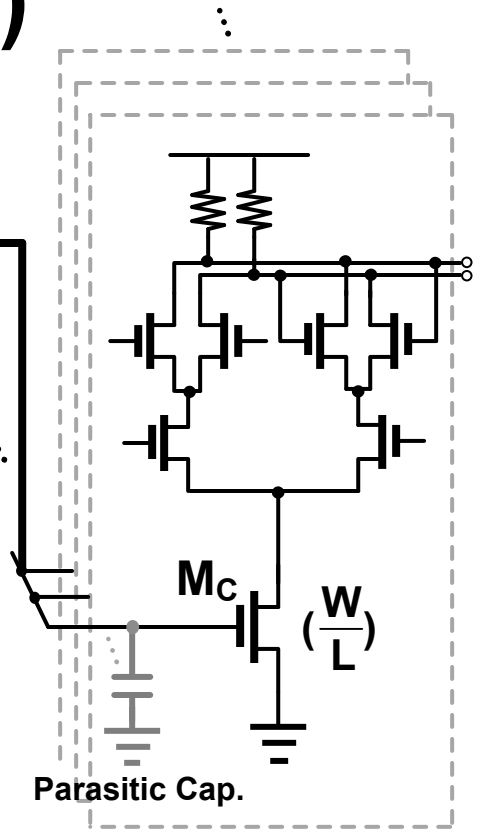


Multi-level & fast mode transition for power saving

Proposed Multi-level Momentarily Activated Bias (M^2AB)





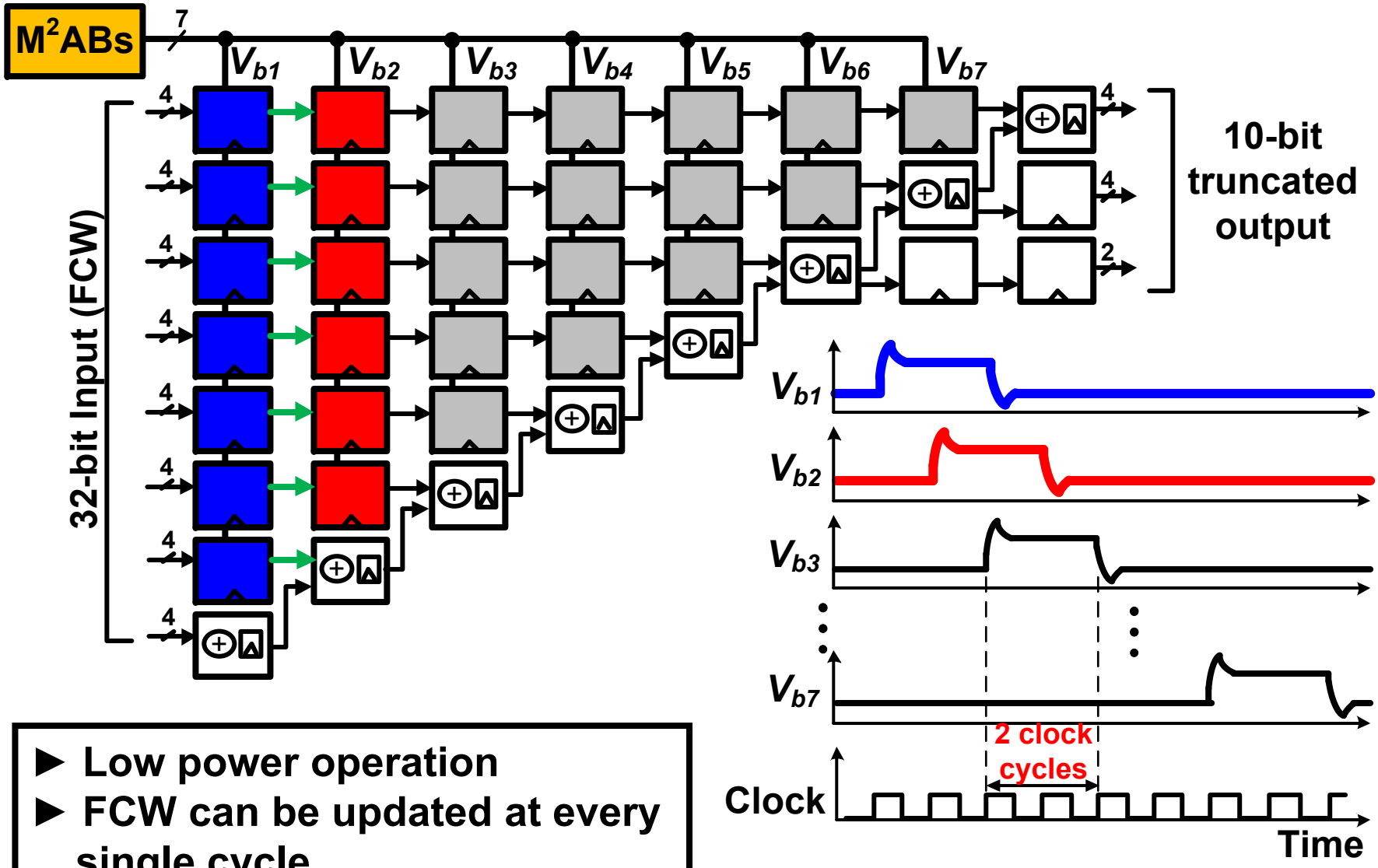


Φ_1 : Sleep mode
Φ_2 : Rapidly waking-up mode
Φ_3 : Normal operation mode
Φ_4 : Quickly turning-off mode

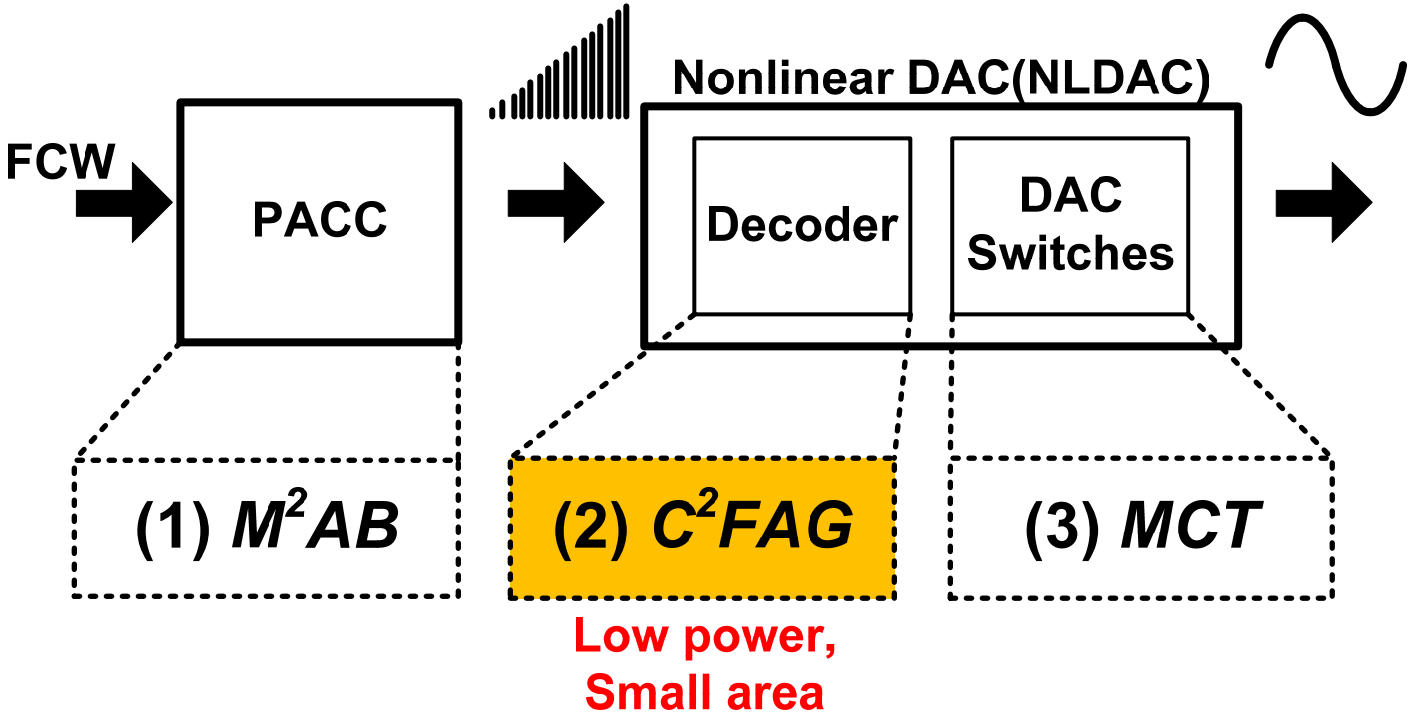
Multi-level Momentarily Activated Bias (M^2AB)

Latches in pre-skewing F/Fs

PACC with M²AB



- Low power operation
- FCW can be updated at every single cycle

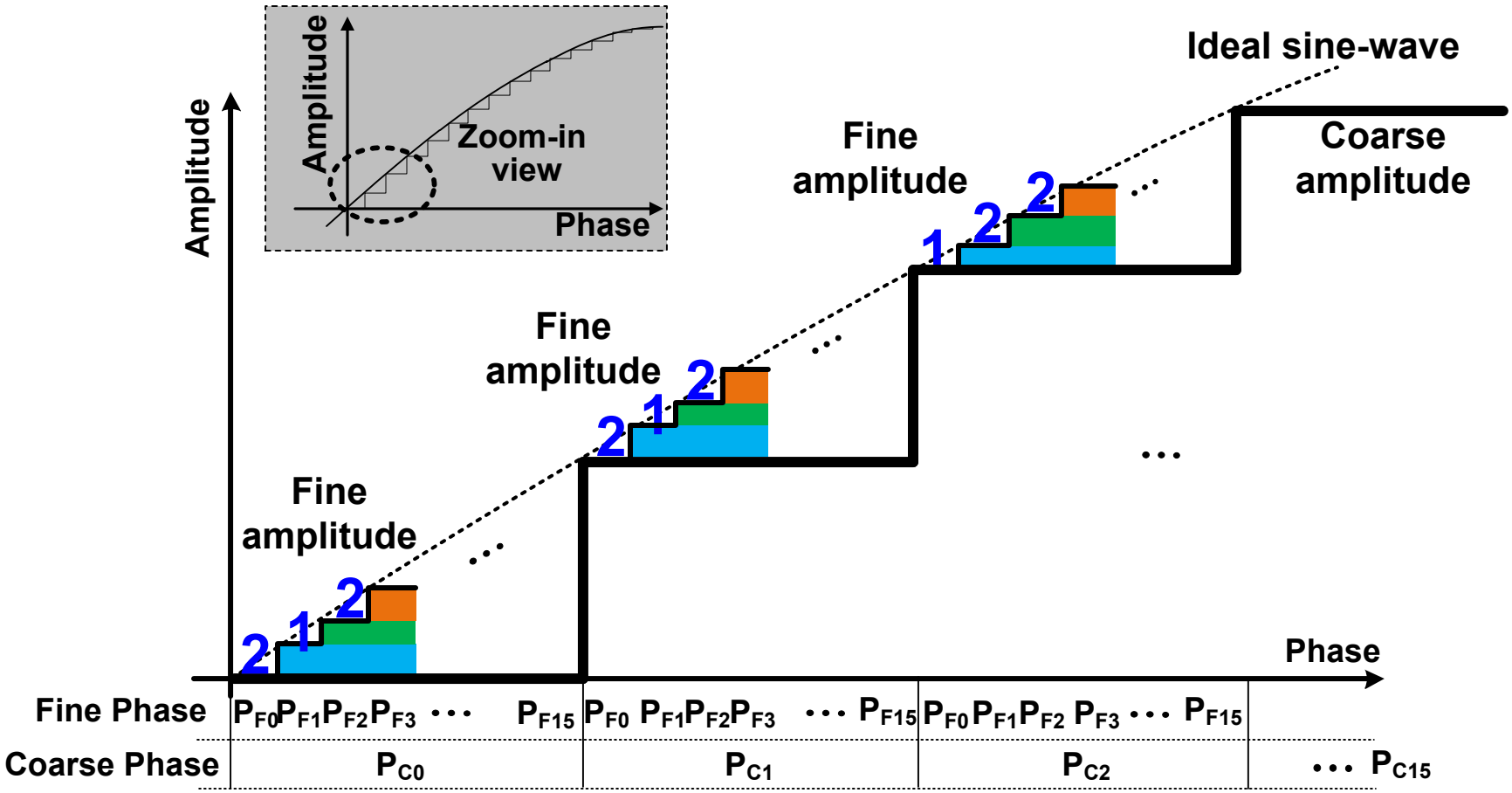


(1) *M²AB* : Multi-level Momentarily Activated Bias

(2) *C²FAG* : Coarse phase-based Consecutive Fine Amplitude Grouping

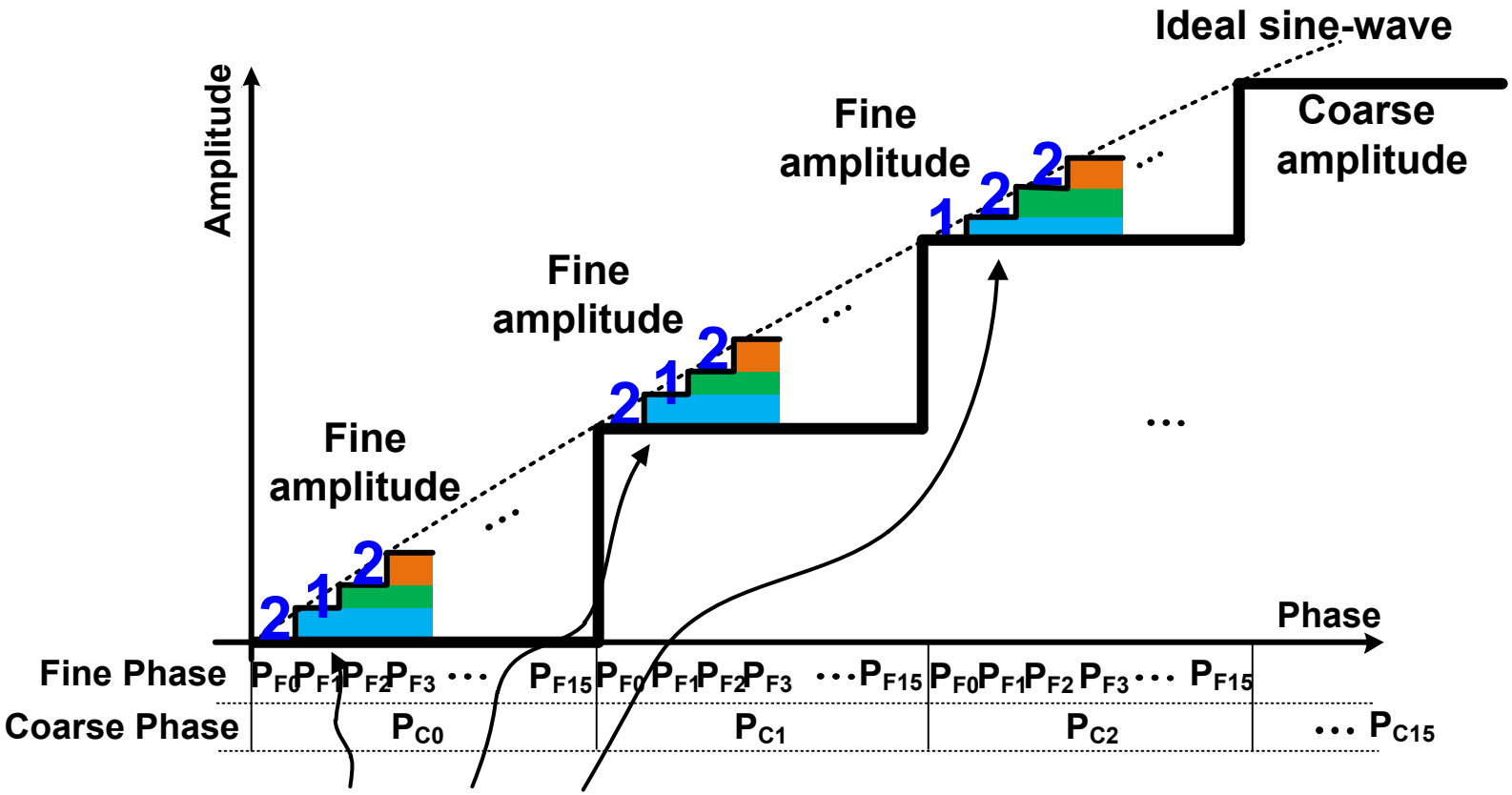
(3) *MCT* : Mixed-wave Conversion Topology

Conventional Segmented NLDAC



Complex relationship between coarse & fine amplitude

Conventional Fine Decoding



Fine \ Coarse	P_{C0}	P_{C1}	P_{C2}	P_{C3}	P_{C4}	P_{C5}	P_{C6}
P_{F3}	2	2	2	2	1	2	1
P_{F2}	1	1	2	1	2	1	2
P_{F1}	2	2	1	2	1	1	1

Conventional decoding for fine amplitude increment

Conventional Fine Decoding

P_{F15}	2	1	2	1	1	1	1	1	1	1	1	0	1	0	0	0
P_{F14}	2	2	1	1	2	2	1	1	1	1	1	1	0	1	1	0
P_{F13}	1	1	2	2	1	1	2	2	1	1	1	0	0	0	0	0
P_{F12}	2	2	1	1	1	1	1	1	1	1	0	1	1	0	0	0
P_{F11}	1	1	2	2	2	2	1	1	1	1	1	1	0	1	0	0
P_{F10}	2	2	1	1	1	1	1	1	1	1	1	0	1	0	0	0
P_{F9}	1	1	2	2	2	1	2	1	1	1	1	1	0	0	1	0
P_{F8}	2	2	1	1	1	2	1	1	2	1	1	1	1	1	0	0
P_{F7}	2	2	1	2	1	1	1	2	1	1	0	1	1	1	1	0
P_{F6}	1	1	1	1	2	2	1	1	1	0	1	1	0	0	0	0
P_{F5}	2	2	2	2	1	1	2	1	1	1	1	1	1	1	1	1
P_{F4}	1	1	1	1	2	1	1	1	1	1	1	0	0	0	0	0
P_{F3}	2	2	2	2	1	2	1	1	1	1	1	1	1	1	0	0
P_{F2}	1	1	2	1	2	1	2	1	1	1	1	1	0	0	0	0
P_{F1}	2	2	1	2	1	1	1	2	1	1	0	1	1	1	1	0
Fine / Coarse	P_{C0}	P_{C1}	P_{C2}	P_{C3}	P_{C4}	P_{C5}	P_{C6}	P_{C7}	P_{C8}	P_{C9}	P_{C10}	P_{C11}	P_{C12}	P_{C13}	P_{C14}	P_{C15}

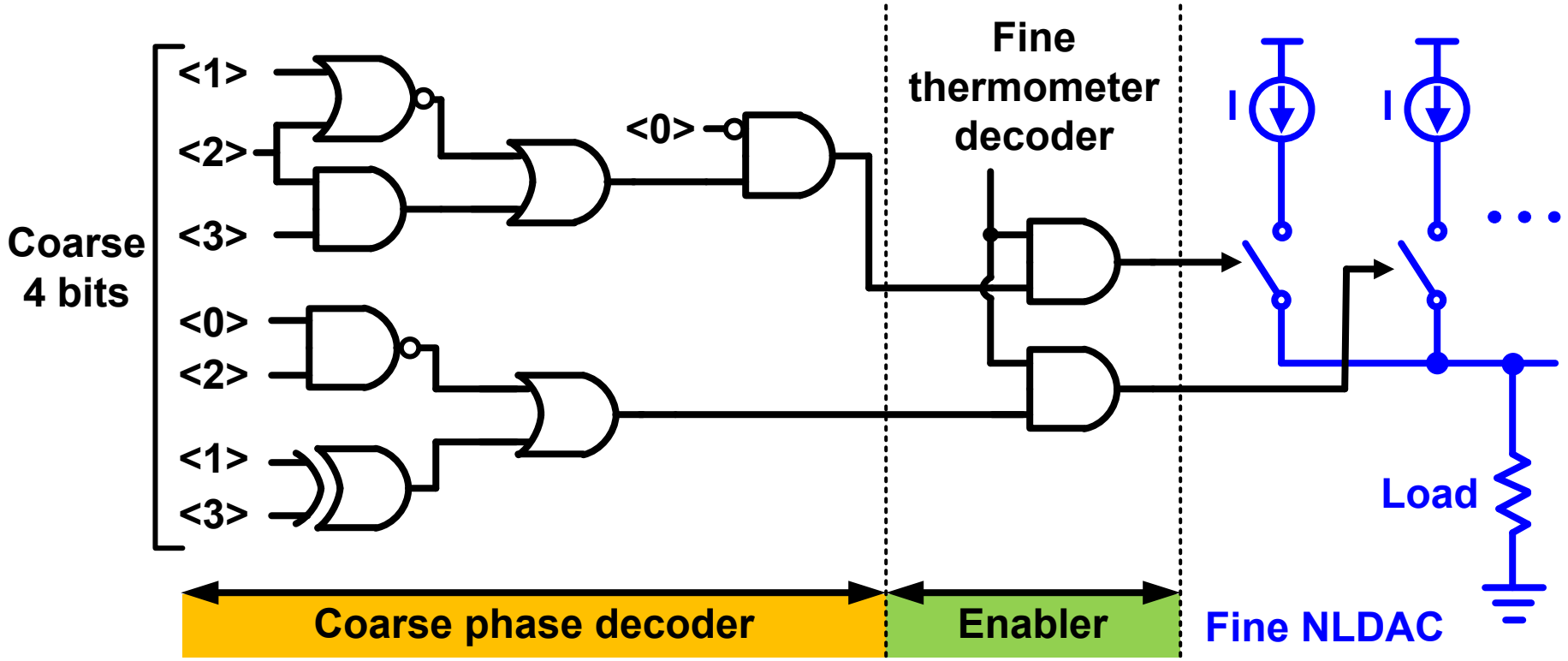
Conventional Fine Decoding

P_{F15}	2	*	1	*	2	*	1	1	1	1	1	1	1	1	*	0	*	1	*	0	0	0
P_{F14}	2	2	*	1	1	*	2	2	*	1	1	1	1	1	1	*	0	*	1	1	*	0
P_{F13}	1	1	*	2	2	*	1	1	*	2	2	*	1	1	1	*	0	0	0	0	0	0
P_{F12}	2	2	*	1	1	1	1	1	1	1	1	1	*	0	*	1	1	*	0	0	0	0
P_{F11}	1	1	*	2	2	2	2	*	1	1	1	1	1	1	*	0	*	1	*	0	0	0
P_{F10}	2	2	*	1	1	1	1	1	1	1	1	1	*	0	*	1	*	0	0	0	0	0
P_{F9}	1	1	*	2	2	2	*	1	*	2	*	1	1	1	1	1	*	0	0	*	1	*	0
P_{F8}	2	2	*	1	1	1	*	2	*	1	1	*	2	*	1	1	1	1	1	*	0	0
P_{F7}	2	2	*	1	*	2	*	1	1	1	*	2	*	1	1	*	0	*	1	1	1	1	*	0
P_{F6}	1	1	1	1	1	*	2	2	*	1	1	1	*	0	*	1	*	1	0	0	0	0	0	0
P_{F5}	2	2	2	2	2	*	1	1	*	2	*	1	1	1	1	1	1	1	1	1	1	1	1	1
P_{F4}	1	1	1	1	1	*	2	*	1	1	1	1	1	1	1	*	0	0	0	0	0	0	0	0
P_{F3}	2	2	2	2	2	*	1	*	2	*	1	1	1	1	1	1	1	1	1	*	0	0	0	0
P_{F2}	1	1	*	2	*	1	*	2	*	1	*	2	*	1	1	1	1	1	*	0	0	0	0	0
P_{F1}	2	2	*	1	*	2	*	1	1	1	*	2	*	1	1	*	0	*	1	1	1	1	*	0
Fine / Coarse	P_{C0}	P_{C1}	P_{C2}	P_{C3}	P_{C4}	P_{C5}	P_{C6}	P_{C7}	P_{C8}	P_{C9}	P_{C10}	P_{C11}	P_{C12}	P_{C13}	P_{C14}	P_{C15}								

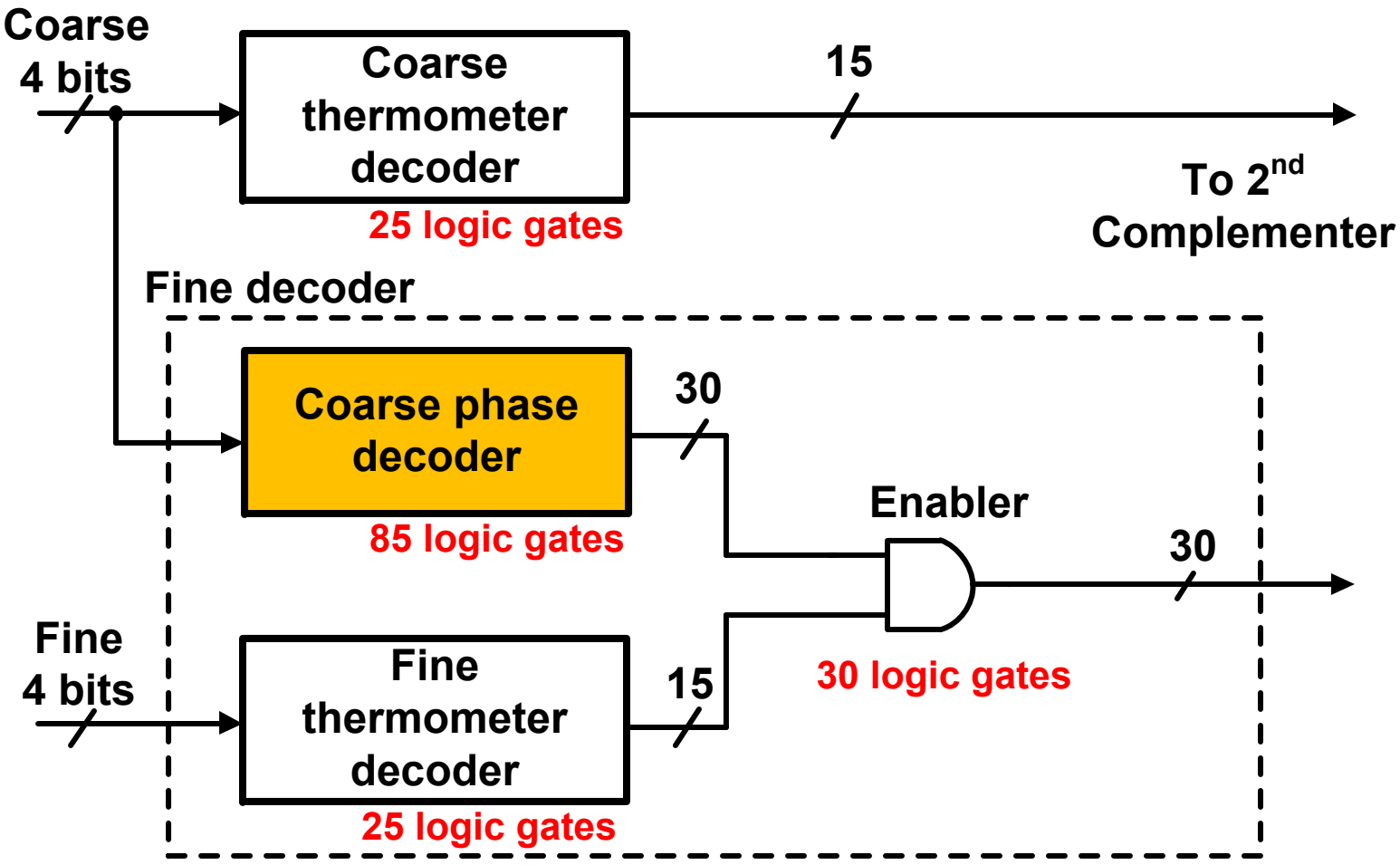
79 positions (*) are required for fine decoding

Conventional Fine Decoding

Coarse / Fine	P_{C0}	P_{C1}	P_{C2}	P_{C3}	P_{C4}	P_{C5}	P_{C6}	P_{C7}	P_{C8}	P_{C9}	P_{C10}	P_{C11}	P_{C12}	P_{C13}	P_{C14}	P_{C15}
P_{F1}	2	2	1	2	1	1	1	2	1	1	0	1	1	1	1	0

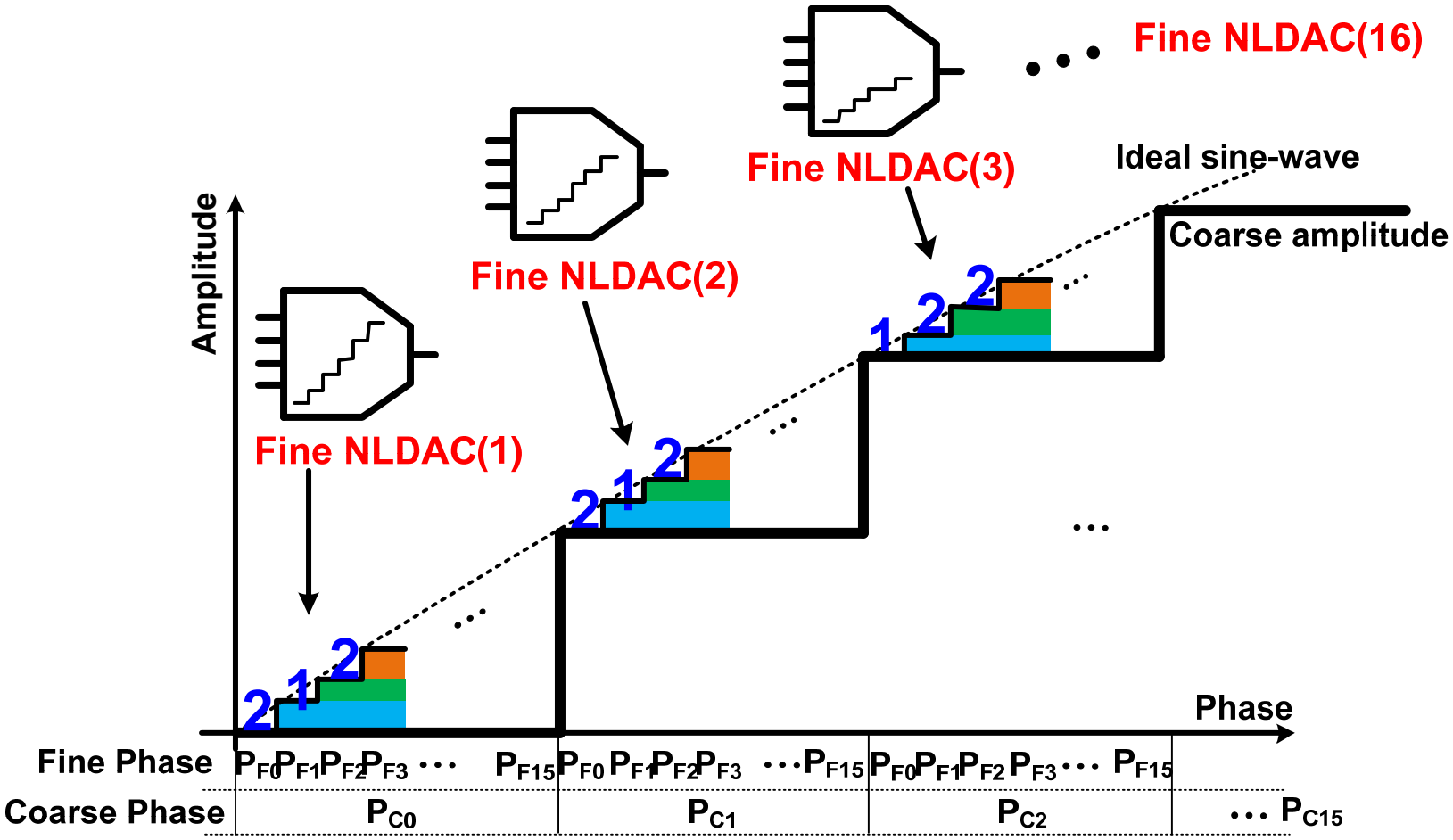


Conventional Decoding Block



- ► total 165 logic gates are required for overall decoding
- ► Coarse phase decoder is most complex part

Multiple fine NLDAC [1]



Multiple fine NLDAC [1]JSSC 2010

- ► Extra area
- ► Mismatches between fine NLDACs

Proposed Decoding with C²FAG

Fine / Coarse	P_{C0}	P_{C1}	P_{C2}	P_{C3}	P_{C4}	P_{C5}	P_{C6}	P_{C7}	P_{C8}	P_{C9}	P_{C10}	P_{C11}	P_{C12}	P_{C13}	P_{C14}	P_{C15}
P_{F15}	2	2	2	2	2	2	2	1	1	1	1	0	0	0	0	0
P_{F14}	2	2	1	1	1	1	1	1	1	1	1	1	1	1	1	0
P_{F13}	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
P_{F12}	2	2	2	2	2	1	1	1	1	1	1	1	1	0	0	0
P_{F11}	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
P_{F10}	2	2	2	2	2	2	2	2	1	1	0	0	0	0	0	0
P_{F9}	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
P_{F8}	2	2	2	2	2	1	1	1	1	1	1	1	0	0	0	0
P_{F7}	2	2	2	2	2	2	2	1	1	1	1	1	1	1	0	0
P_{F6}	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
P_{F5}	2	2	2	1						1	1	1	1	1	1	1
P_{F4}	1	1	1	1						1	1	1	0	0	0	0
P_{F3}	2	2	2	2	2	2	2	2	1	1	1	1	1	1	0	0
P_{F2}	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
P_{F1}	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	0

Descending order →

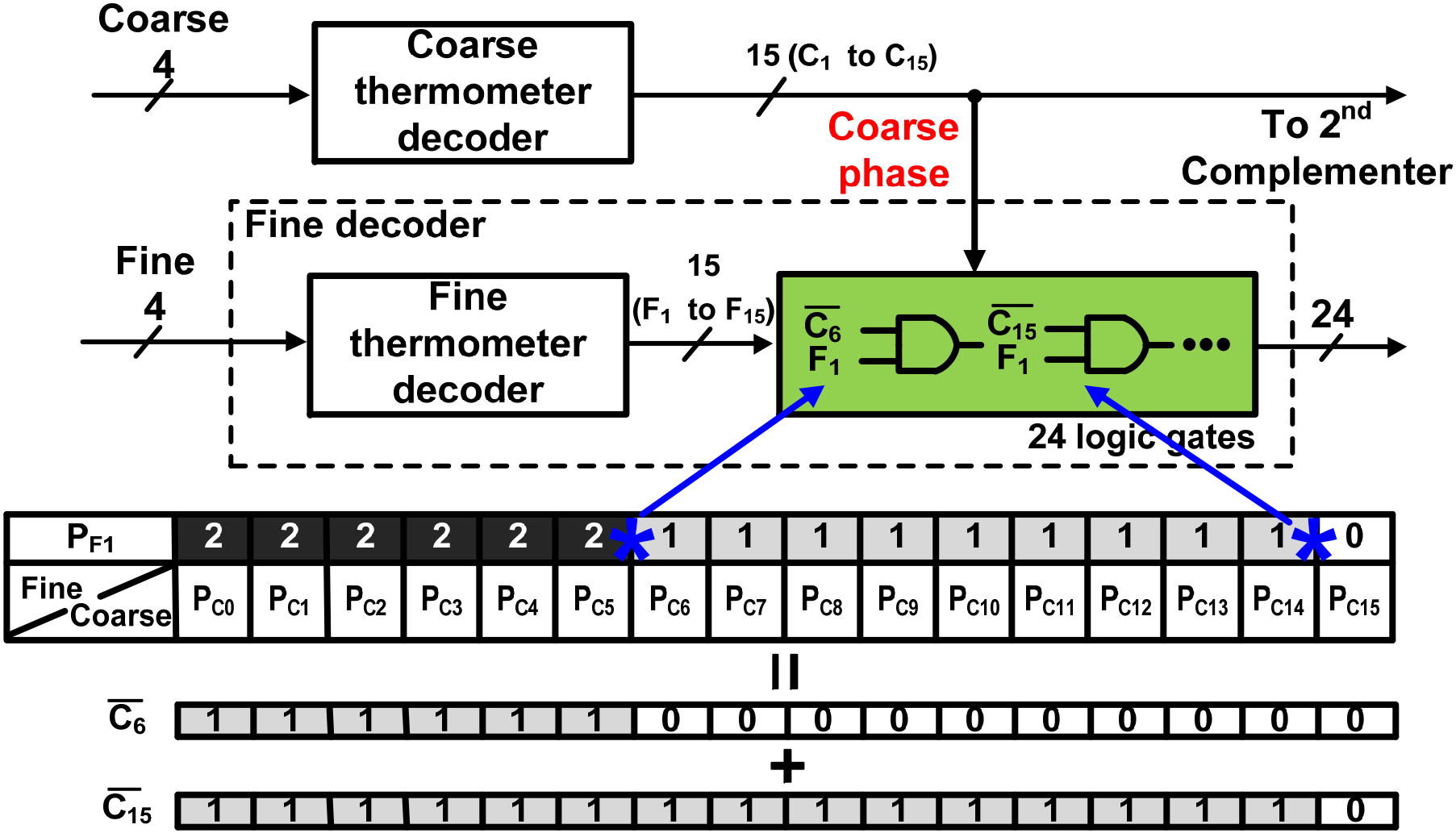
C²FAG : Coarse phase-based Consecutive Fine Amplitude Grouping

Proposed Decoding with C²FAG

P_{F15}	2	2	2	2	2	2	2*	1	1	1	1*	0	0	0	0	0
P_{F14}	2	2*	1	1	1	1	1	1	1	1	1	1	1	1	1*	0
P_{F13}	1	1	1	1	1	1	1	1	1	1	1*	0	0	0	0	0
P_{F12}	2	2	2	2	2*	1	1	1	1	1	1	1	1*	0	0	0
P_{F11}	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1*	0
P_{F10}	2	2	2	2	2	2	2	2*	1	1*	0	0	0	0	0	0
P_{F9}	1	1	1	1	1	1	1	1	1	1	1	1	1*	0	0	0
P_{F8}	2	2	2	2	2*	1	1	1	1	1	1	1*	0	0	0	0
P_{F7}	2	2	2	2	2	2	2*	1	1	1	1	1	1	1*	0	0
P_{F6}	1	1	1	1	1	1	1	1	1	1*	0	0	0	0	0	0
P_{F5}	2	2	2*	1	1	1	1	1	1	1	1	1	1	1	1	1
P_{F4}	1	1	1	1	1	1	1	1	1	1	1	1*	0	0	0	0
P_{F3}	2	2	2	2	2	2	2	2*	1	1	1	1	1	1*	0	0
P_{F2}	1	1	1	1	1	1	1	1	1	1	1*	0	0	0	0	0
P_{F1}	2	2	2	2	2	2*	1	1	1	1	1	1	1	1	1*	0
Fine / Coarse	P_{C0}	P_{C1}	P_{C2}	P_{C3}	P_{C4}	P_{C5}	P_{C6}	P_{C7}	P_{C8}	P_{C9}	P_{C10}	P_{C11}	P_{C12}	P_{C13}	P_{C14}	P_{C15}

23 Positions (*) are required for fine decoding

Decoder with C²FAG

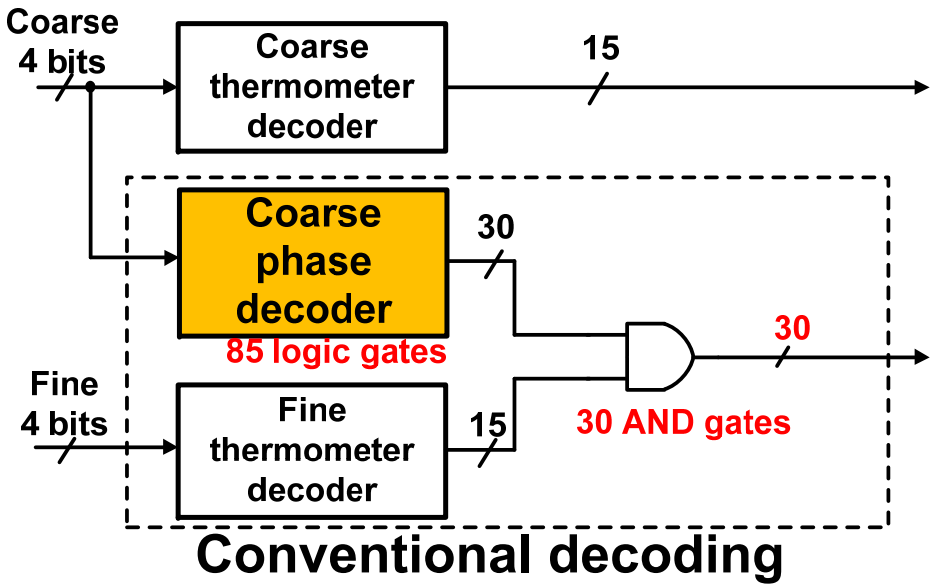


- Coarse phase decoder is completely removed
- Power consumption is reduced & speed is increased

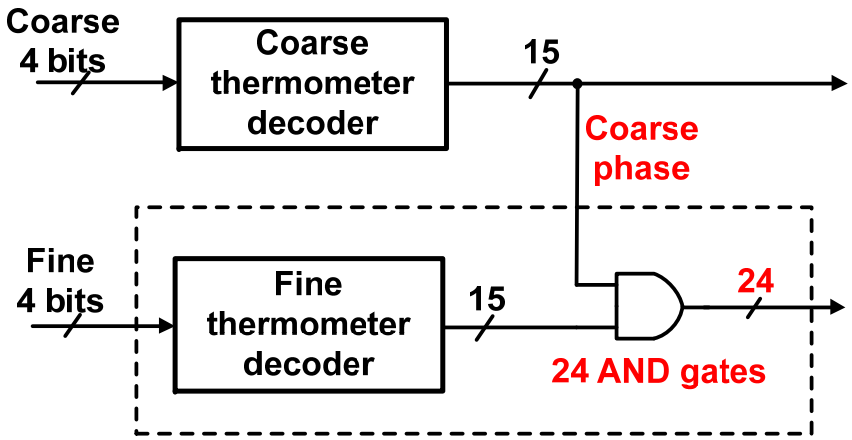
Conventional Vs. C²FAG

	P_{C0}	P_{C1}	P_{C2}	P_{C3}	P_{C4}	P_{C5}	P_{C6}	P_{C7}	P_{C8}	P_{C9}	P_{C10}	P_{C11}	P_{C12}	P_{C13}	P_{C14}	P_{C15}
P_{F15}	2	1	2	1	1	1	1	1	1	1	1	0	1	0	0	0
P_{F14}	2	2	1	1	2	2	1	1	1	1	1	1	0	1	1	0
P_{F13}	1	1	2	2	1	1	2	2	1	1	1	0	0	0	0	0
P_{F12}	2	2	1	1	1	1	1	1	1	1	0	1	1	0	0	0
P_{F11}	1	1	2	2	2	2	1	1	1	1	1	1	0	1	0	0
P_{F10}	2	2	1	1	1	1	1	1	1	1	1	0	1	0	0	0
P_{F9}	1	1	2	2	2	1	2	1	1	1	1	1	0	0	1	0
P_{F8}	2	2	1	1	1	2	1	1	2	1	1	1	1	0	0	0
P_{F7}	2	2	1	2	1	1	1	2	1	1	0	1	1	1	1	0
P_{F6}	1	1	1	1	2	2	1	1	1	0	1	1	0	0	0	0
P_{F5}	2	2	2	2	1	1	2	1	1	1	1	1	1	1	1	1
P_{F4}	1	1	1	1	2	1	1	1	1	1	1	0	0	0	0	0
P_{F3}	2	2	2	2	1	2	1	1	1	1	1	1	1	1	0	0
P_{F2}	1	1	2	1	2	1	2	1	1	1	1	1	0	0	0	0
P_{F1}	2	2	1	2	1	1	1	2	1	1	0	1	1	1	1	0
Fine / Coarse	P_{C0}	P_{C1}	P_{C2}	P_{C3}	P_{C4}	P_{C5}	P_{C6}	P_{C7}	P_{C8}	P_{C9}	P_{C10}	P_{C11}	P_{C12}	P_{C13}	P_{C14}	P_{C15}

	P_{C0}	P_{C1}	P_{C2}	P_{C3}	P_{C4}	P_{C5}	P_{C6}	P_{C7}	P_{C8}	P_{C9}	P_{C10}	P_{C11}	P_{C12}	P_{C13}	P_{C14}	P_{C15}
P_{F15}	2	2	2	2	2	2	2	1	1	1	1	0	0	0	0	0
P_{F14}	2	2	1	1	1	1	1	1	1	1	1	1	1	1	1	0
P_{F13}	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
P_{F12}	2	2	2	2	2	1	1	1	1	1	1	1	0	0	0	0
P_{F11}	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
P_{F10}	2	2	2	2	2	2	2	2	1	1	0	0	0	0	0	0
P_{F9}	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
P_{F8}	2	2	2	2	2	1	1	1	1	1	1	0	0	0	0	0
P_{F7}	2	2	2	2	2	2	1	1	1	1	1	1	0	0	0	0
P_{F6}	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
P_{F5}	2	2	2	1	1	1	1	1	1	1	1	1	1	1	1	1
P_{F4}	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
P_{F3}	2	2	2	2	2	2	2	2	1	1	1	1	1	0	0	0
P_{F2}	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
P_{F1}	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	0
Fine / Coarse	P_{C0}	P_{C1}	P_{C2}	P_{C3}	P_{C4}	P_{C5}	P_{C6}	P_{C7}	P_{C8}	P_{C9}	P_{C10}	P_{C11}	P_{C12}	P_{C13}	P_{C14}	P_{C15}

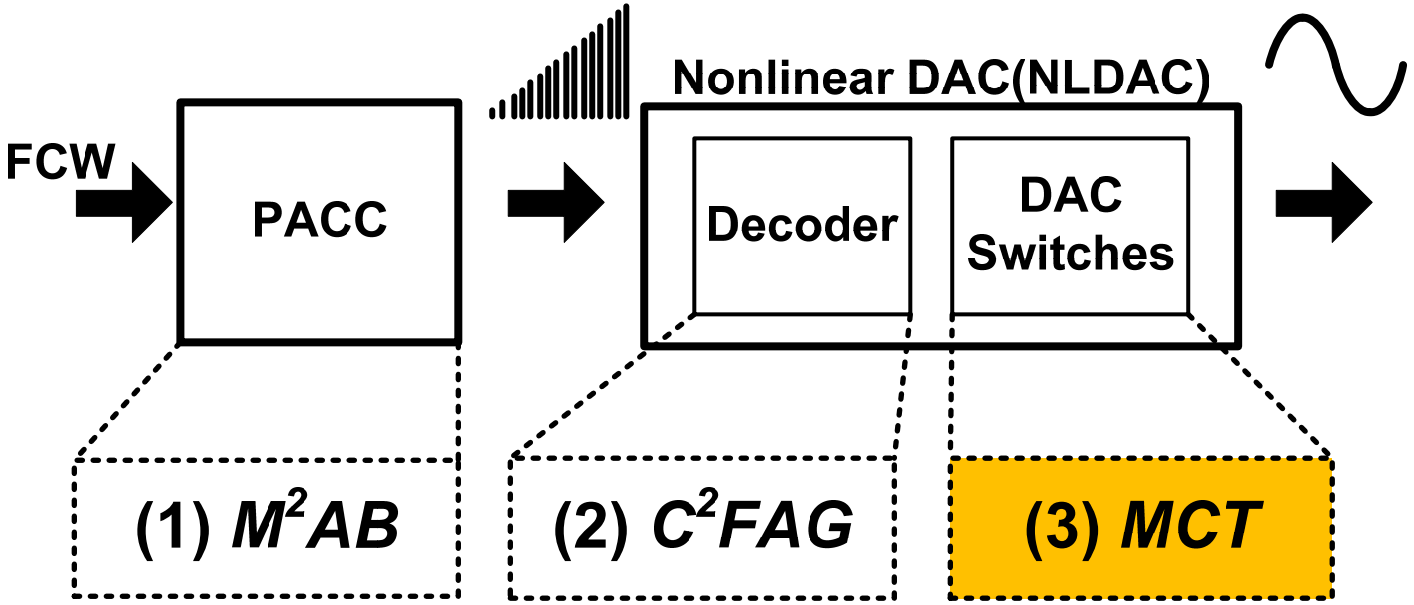


Conventional decoding



Proposed C²FAG

C²FAG reduces decoder complexity by more than 50%

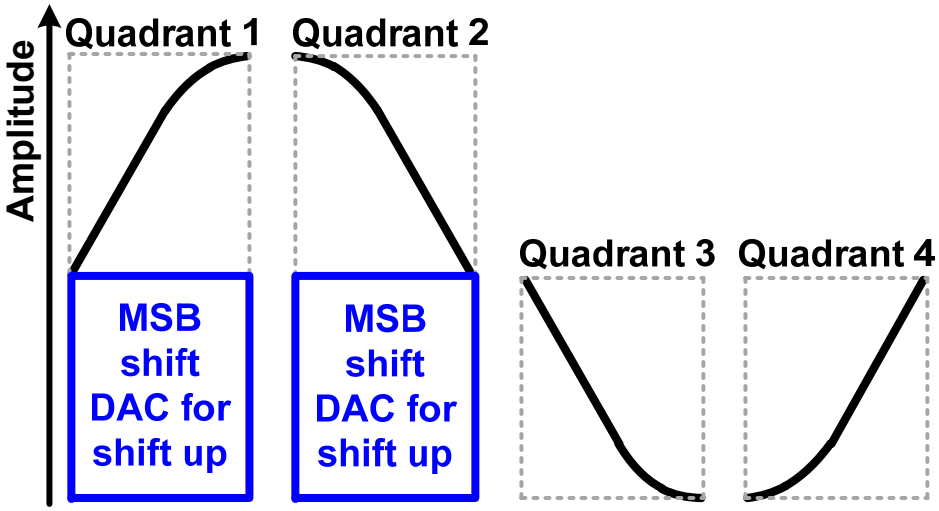


(1) *M²AB* : Multi-level Momentarily Activated Bias

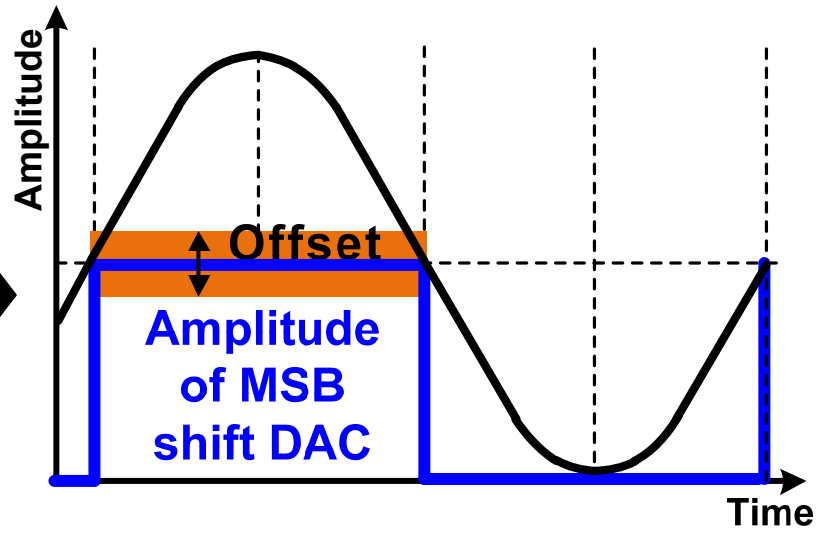
(2) *C²FAG* : Coarse phase-based Consecutive Fine Amplitude Grouping

(3) *MCT* : Mixed-wave Conversion Topology

Conventional Quarter Sine-wave Technique



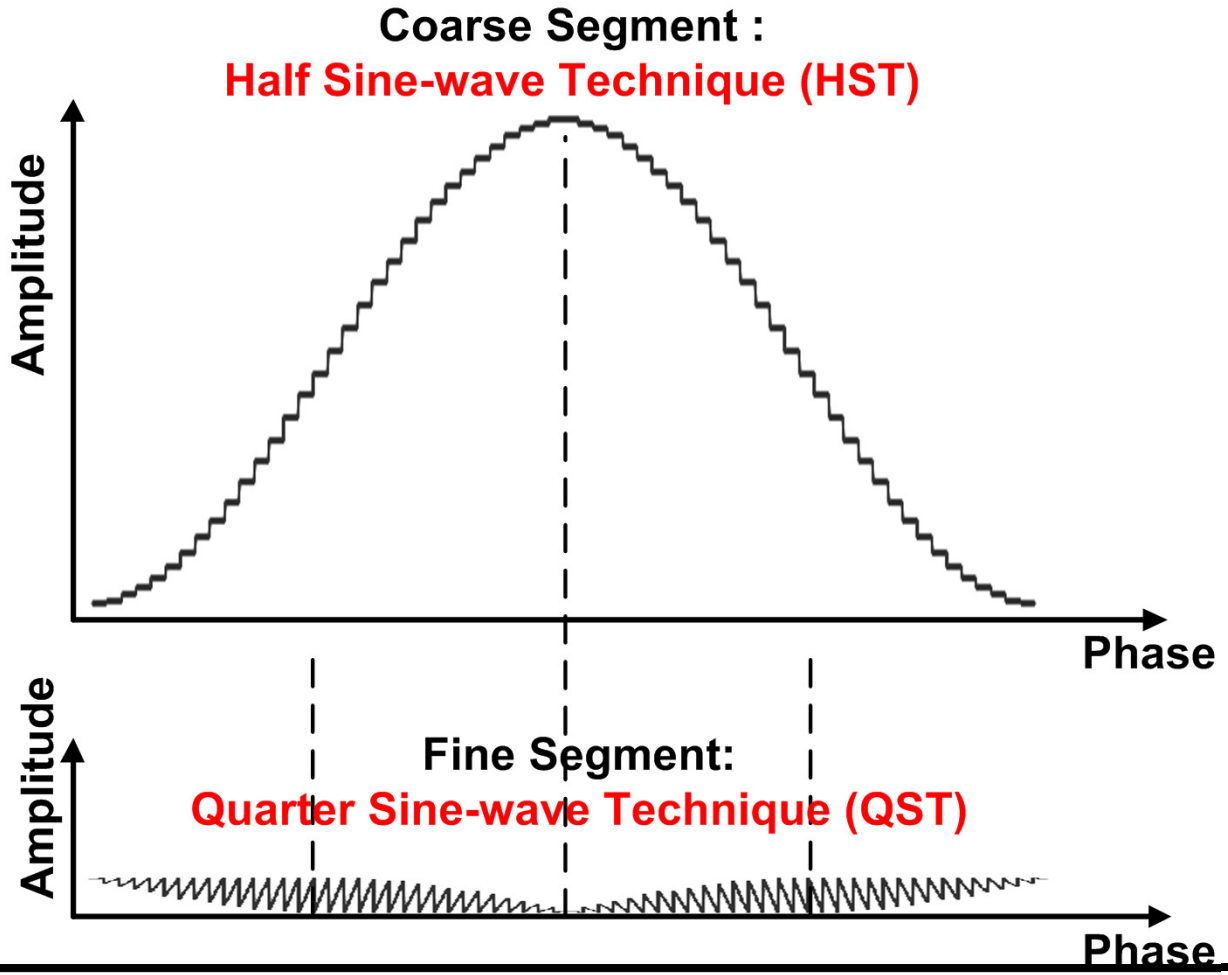
Conventional Quarter Sine-wave Technique (QST) with NLDAC



Synthesized sine-wave

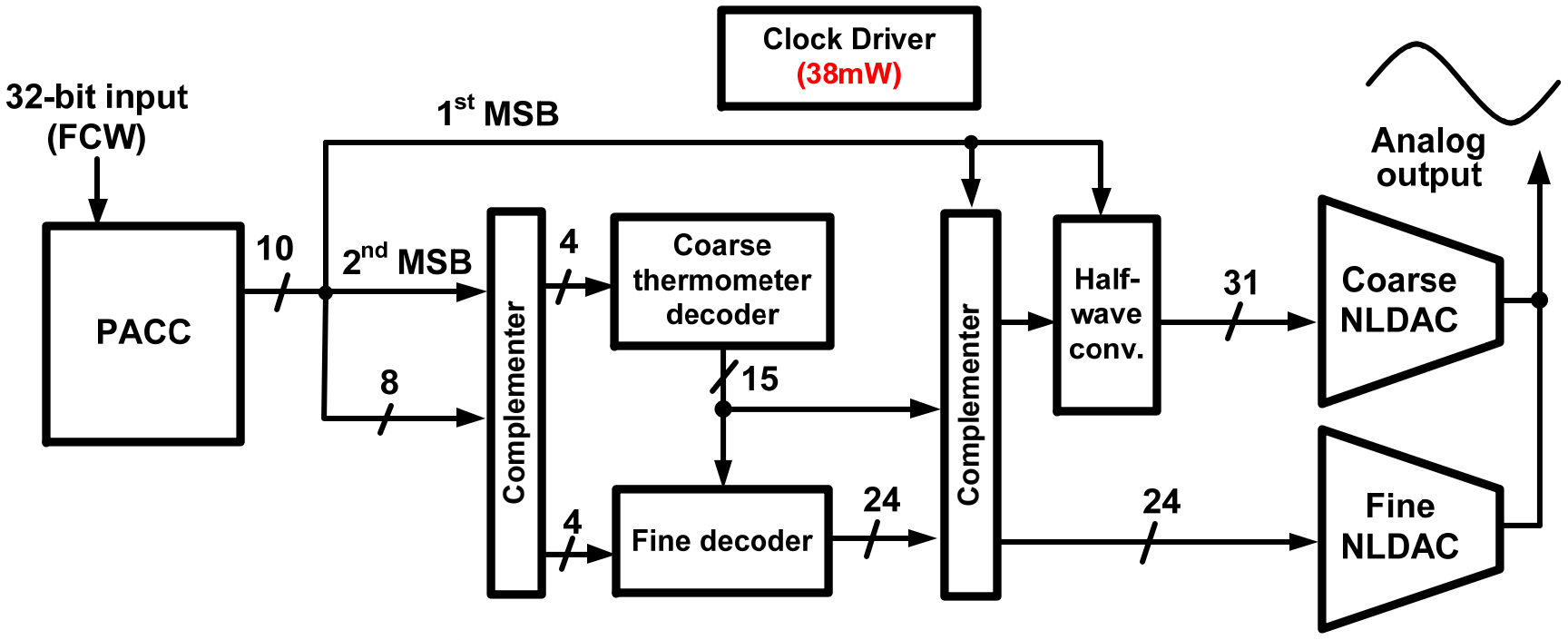
MSB shift DAC can cause significant harmonic distortions

Proposed Mixed-wave Conversion Topology (MCT)

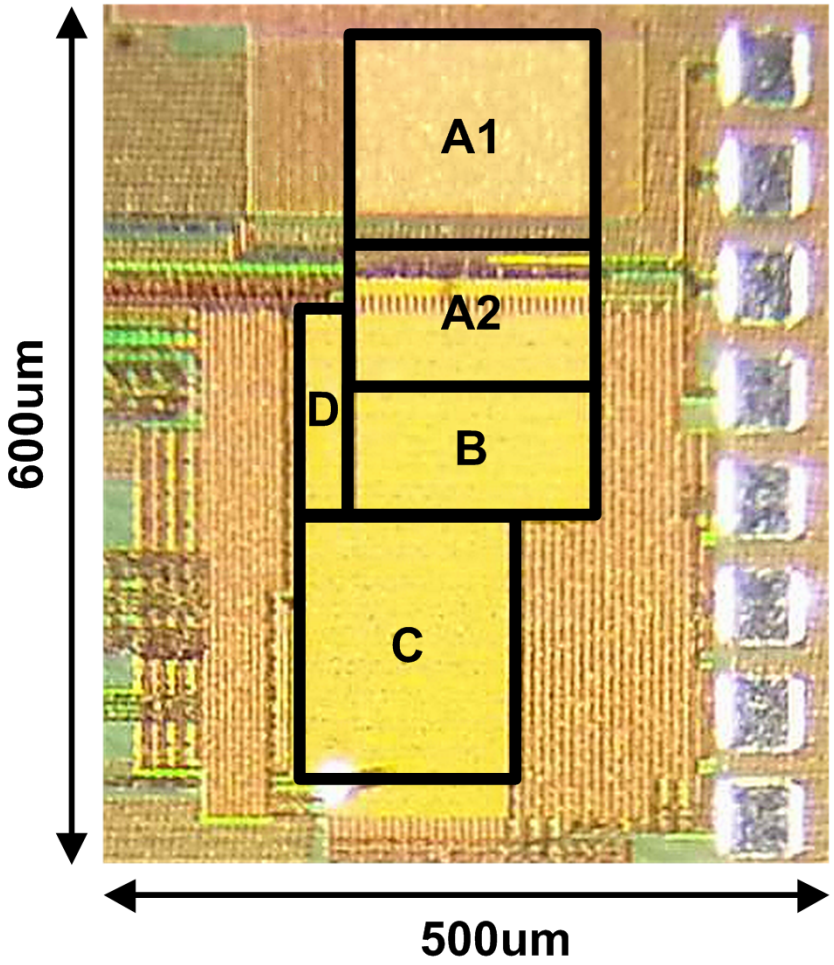


Mixed-wave Conversion Topology (MCT) is the hybrid-type conversion with HST and QST

Detailed Block Diagram



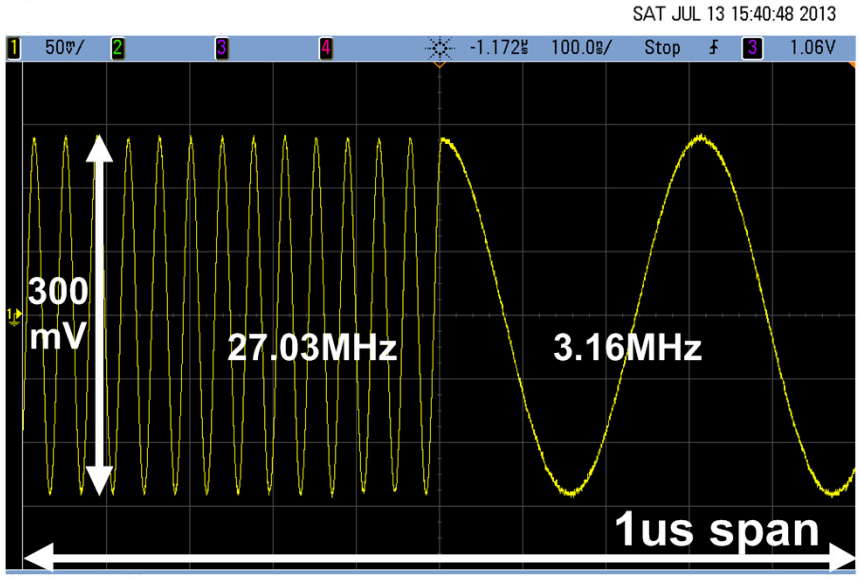
Chip Micrograph

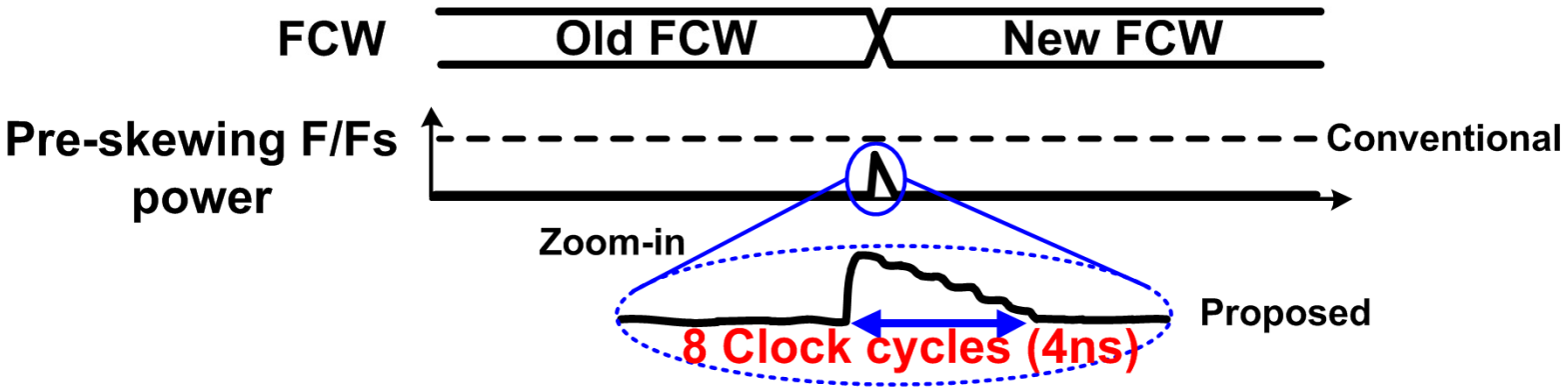


AREA	NAME
A1	Current source array
A2	Current switches & driver
B	Decoder
C	Phase accumulator
D	Clock driver

Measured Time Domain Signal

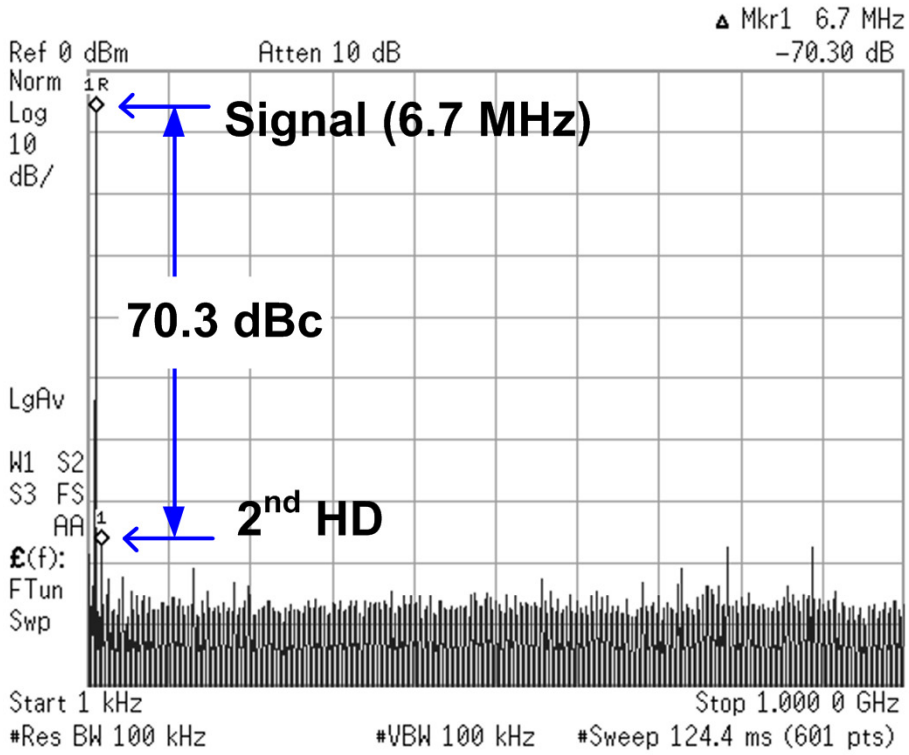
Single ended output

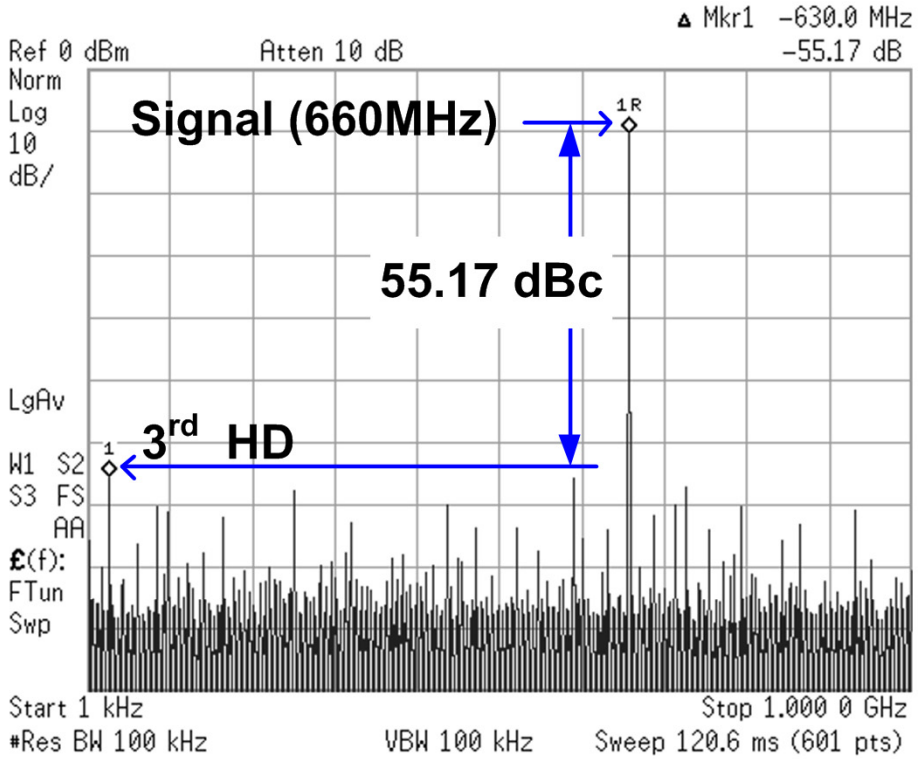




Pre-skewing F/Fs are active only for 4ns
Switching time (latency) : 5ns (10clock cycles)

Measured Spectra



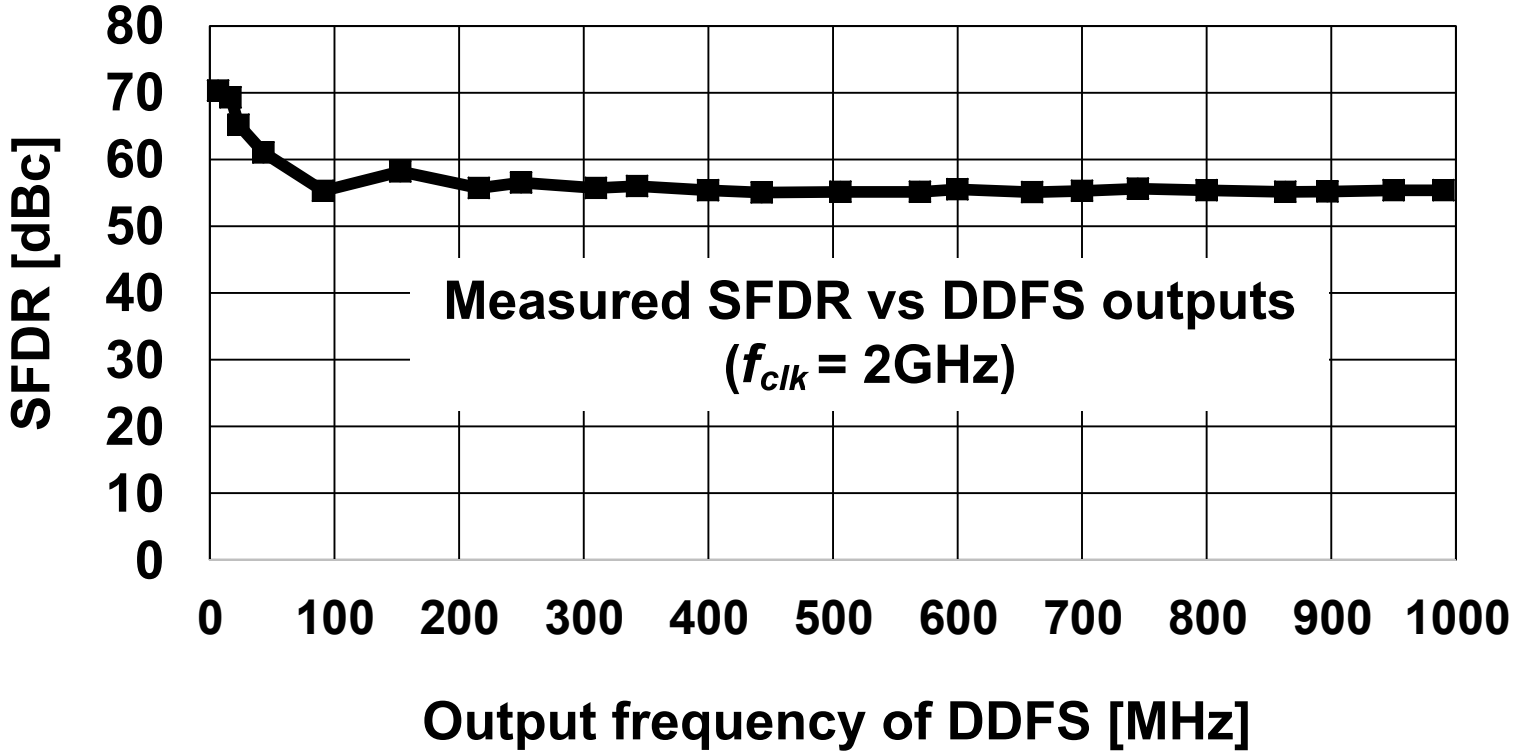


Best SFDR = 70.3 dBc
SINAD = 54.6 dB (8.8 bit ENOB)

Worst SFDR = 55.17 dBc
SINAD = 45.1 dB (7.2 bit ENOB)

Amplitude resolution of proposed DDFS : 9 bit

SFDR of Various Output Freq.



Minimum SFDR is 55.17 dBc when clocked at 2GHz

Performance Summary

DDFS with on-chip DAC	[1] JSSC 2010	[2] JSSC 2010	[3] JSSC 2011	This work
Technology	SiGe 200/250 GHz f_T/f_{MAX}	90nm CMOS	0.35um SiGe BiCMOS	55nm CMOS
Input (FCW) width [bits]	11	24	9	32
Clock frequency [GHz]	8.6	1.3	5	2
Frequency tuning step [Hz]	4.2×10^6	77	9.7×10^6	0.46
Amplitude resolution [bits]	10	11	8	9
Supply voltage (digital/analog) [V]	3.3 / 3.3	1.2 / 2.5	3.3 / 3.3	1 / 2.5
Power consumption [W]	4.8	0.35	0.46	0.13
Power Efficiency [W/GHz]	0.56	0.27	0.092	0.065
Max. output current [mA]	14.8	16	N/A	12
Load resistance [Ω]	15	50	N/A	50
$SFDR_{best}$ [dBc]	50	55	48.7	70.3
$SFDR_{worst}$ [dBc]	33	52	45.7	55.17
Active area [mm^2]	7.5	0.9	2.1	0.1

Performance Summary

	[1] JSSC 2010	[2] JSSC 2010	[3] JSSC 2011	This work
Technology	SiGe 200/250 GHz f_T/f_{MAX}	90nm CMOS	0.35um SiGe BiCMOS	55nm CMOS
Structure	Segmented NLDAC	Segmented NLDAC (Hybrid)	Linear DAC with Triangle-to-sine converter	Segmented NLDAC (PACC with M^2AB + C^2FAG+MCT)
FOM_1	81	1509	2133	8944
FOM_2	10.8	1677	1016	89442
FOM_3 ($x10^3$)	16.9	565	N/A	19674

x4.1 x53.3 x34.8

FOM_1	FOM_2	FOM_3
$\frac{2^{SFDR_{worst}/6} \times f_{clk}}{P_{total}}$	$\frac{FOM_1}{\text{Active area}}$	$\frac{2^{(SFDR_{Best}-1.76)/6} \times 2^{(SFDR_{Worst}-1.76)/6} \times f_{clk}}{P_{total} - 0.5 \cdot I_{Load}^2 \times R_{Load}}$

Conclusion

- **Three key ideas (M^2AB, C^2FAG, MCT) are developed for enhancing overall performances of the DDFS.**

- **Proposed DDFS design allows for high speed operation with low power and small area while maintaining good conversion accuracy.**

A 42mW 230fs-Jitter Sub-sampling 60GHz PLL in 40nm CMOS

Viki Szortyka[1,2], Qixian Shi[1,2], Kuba Raczkowski[1], Bertrand Parvais[1], Maarten Kuijk[2] and Piet Wambacq[1,2]

[1]imec, Leuven, Belgium

[2]Vrije Universiteit Brussel, Brussels, Belgium

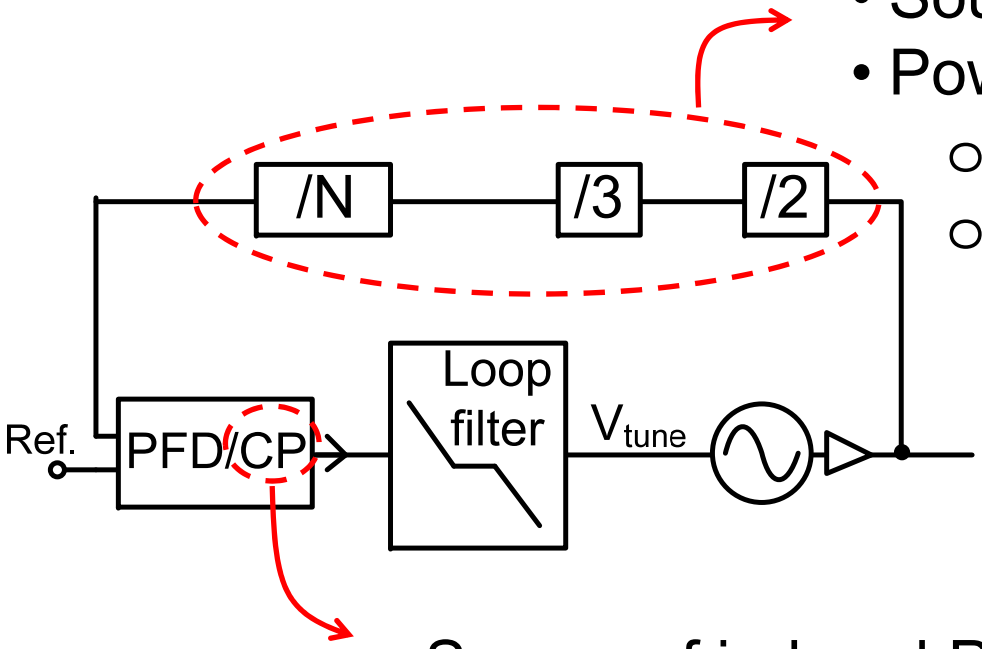
Outline

- Motivation
- mm-Wave sub-sampling PLL
- PLL architecture
  - QVCO
  - Dividers
  - Sub-sampling part
- Measurement results
- Summary

Motivation

- PLL for high data rate communication @57-66GHz
- Quadrature outputs for direct conversion
- Low integrated PN → TX EVM < -21dB for 16QAM

Limitations of classical PFD/CP PLL



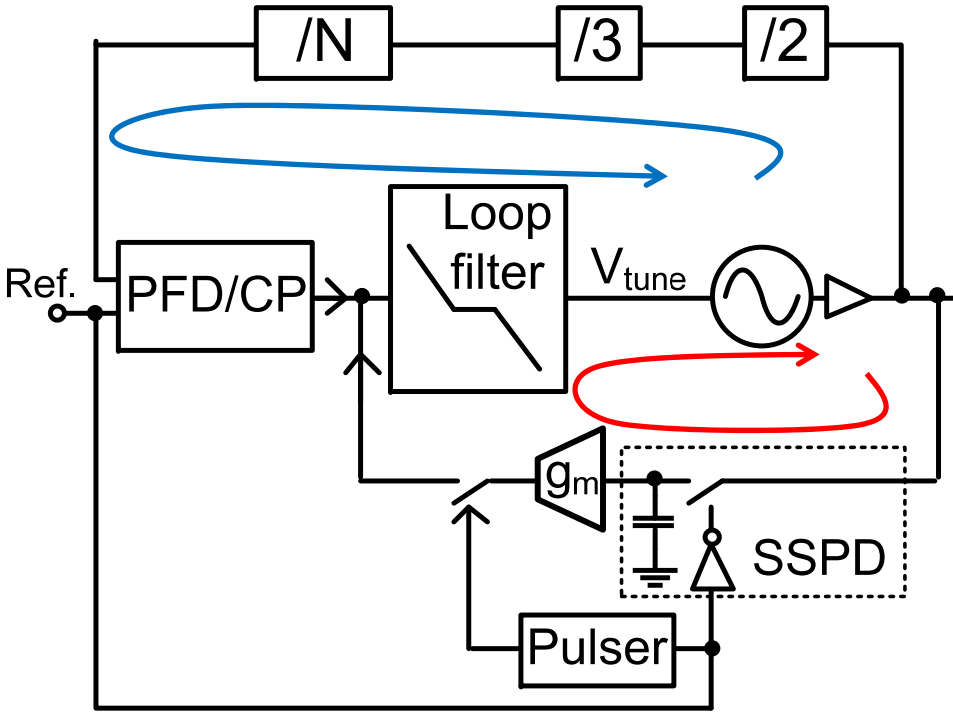
- Source of in-band PN
- Power consumption
  - Low-jitter
  - Cover 60GHz channels (PVT)

- Source of in-band PN → extra P_{DC}

Sub-sampling PLL (SSPLL)

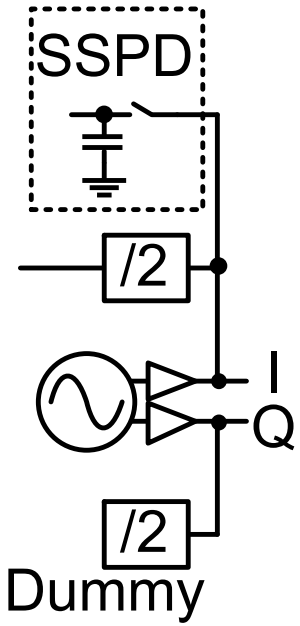
Classical PFD/CP *FLL:*
- Only for frequency acquisition
- Powered down in SSPLL mode

[Gao, ISSCC 2009]

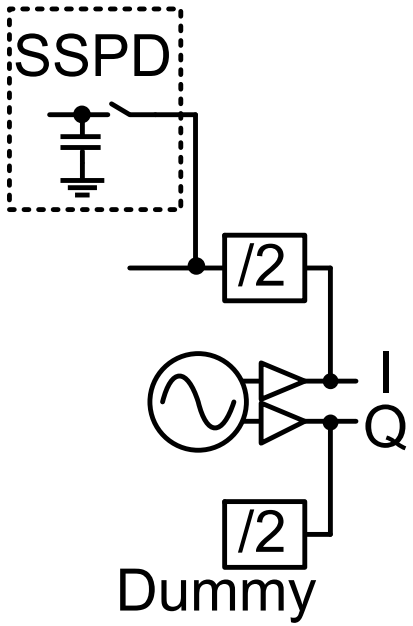


Subsampling PLL
- Sub-sampling phase detector (SSPD)
- Div noise eliminated
- g_m << CP noise
- P_{DC} is reduced:
  - ~~Divider chain~~
  - ~~CP~~

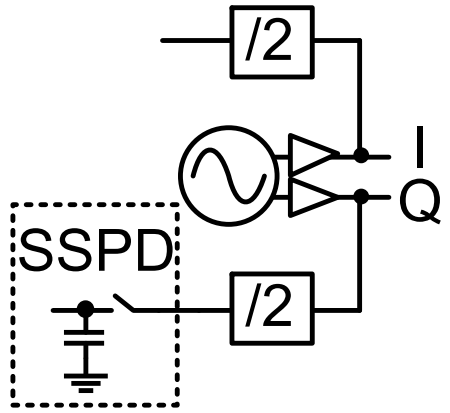
Introducing sub-sampling in a mm-Wave PLL



- Loading @ 60GHz
- Decreased swing

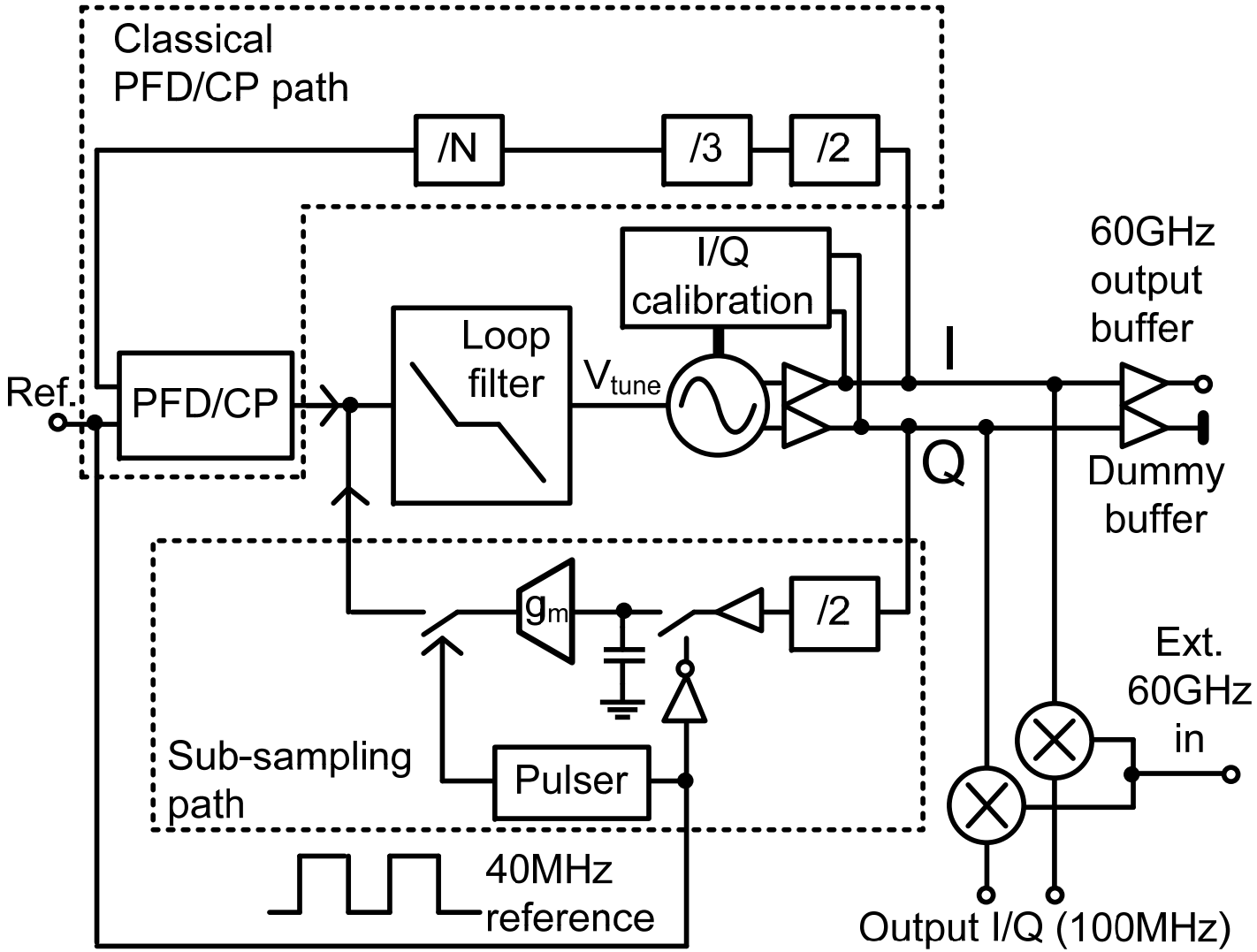


- Lower freq. (30GHz)
- Extra loading of the divider



- I/Q outputs used
- No extra C_{LOAD}
- No extra P_{DC}
- Our solution

PLL architecture



Outline

- Motivation
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  - Dividers
  - Sub-sampling part
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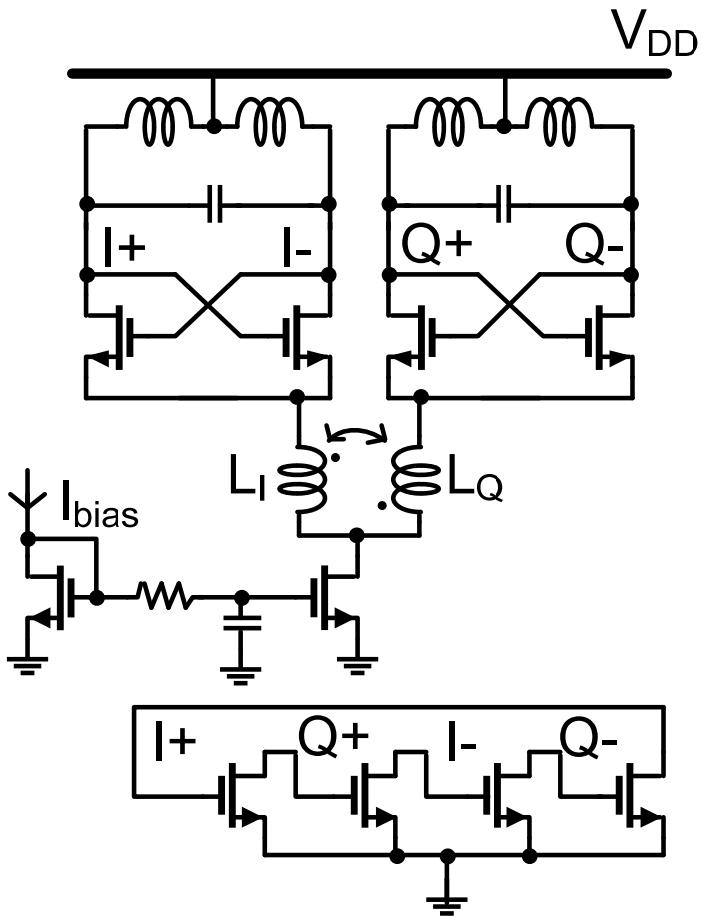
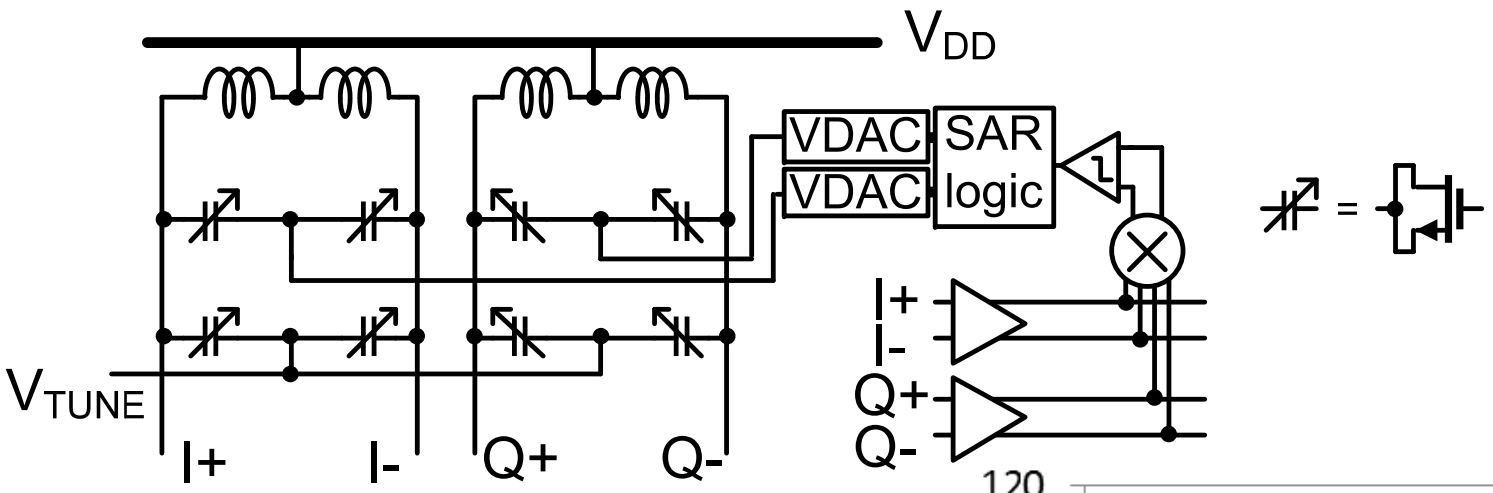
QVCO uses super-harmonic coupling

- Good phase noise
- Wide tuning range
- Relaxed headroom

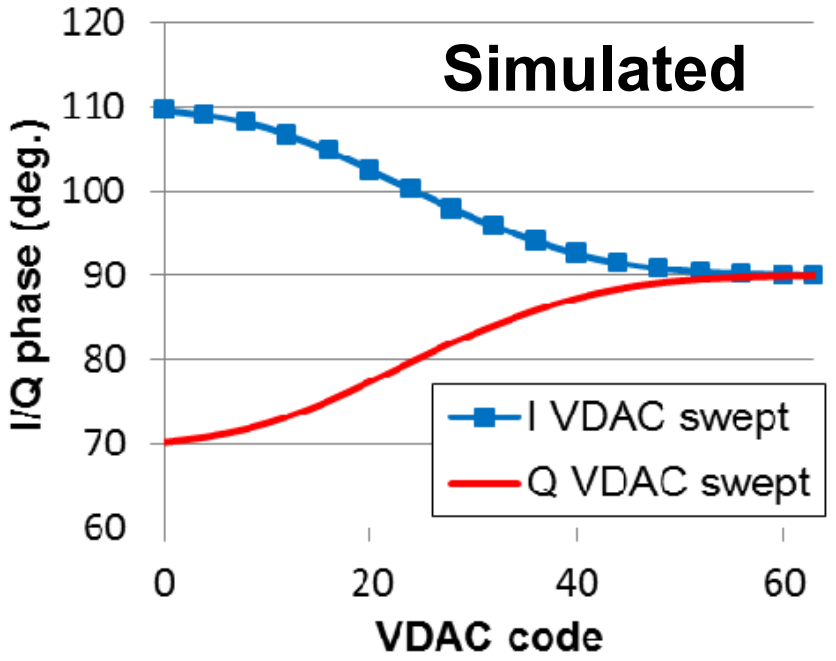
- Weak coupling
- Larger quadrature error



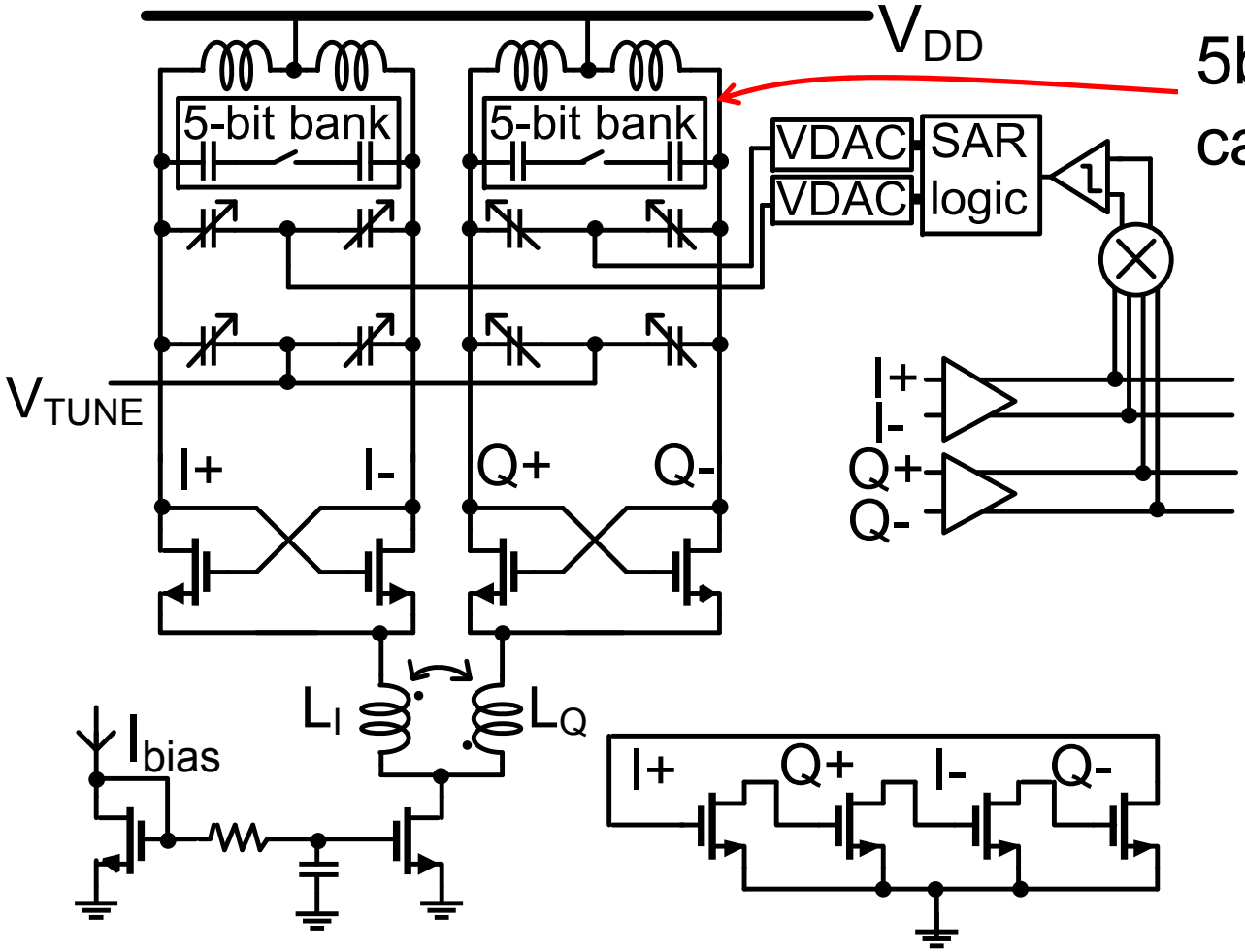
I/Q phase is calibrated



- Mixer output ~ φ_{error}
- 6b VDACs tune the phase
- SAR loop minimizes φ_{error}



QVCO covers 9GHz tuning range



5b coarse tuning capacitor bank

K_{VCO}≈1GHz/V: low enough for PN, high enough to stay in lock

Outline

- Motivation
- mm-Wave sub-sampling PLL
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  - QVCO
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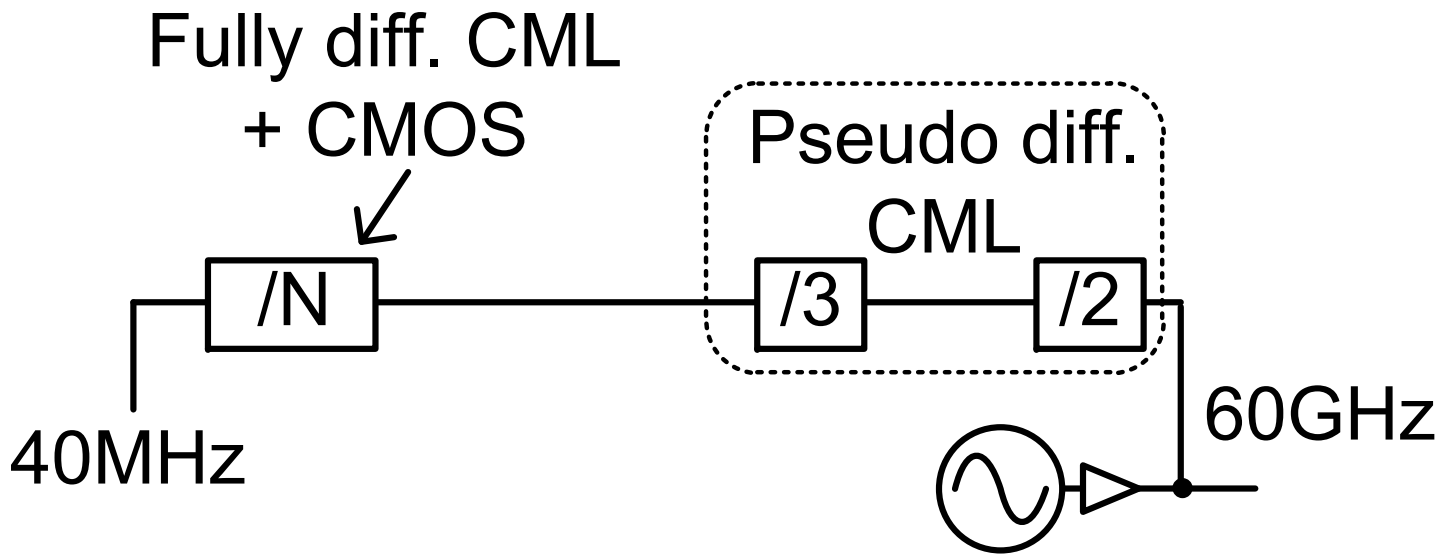
Division chain

- Integer-N
- Widely used f_{REF} (40MHz) → lower system cost
- Target channels: 58.32, 60.48, 62.64 and 64.8GHz
- Static/CML preferred over inj. locked for robustness



Outline

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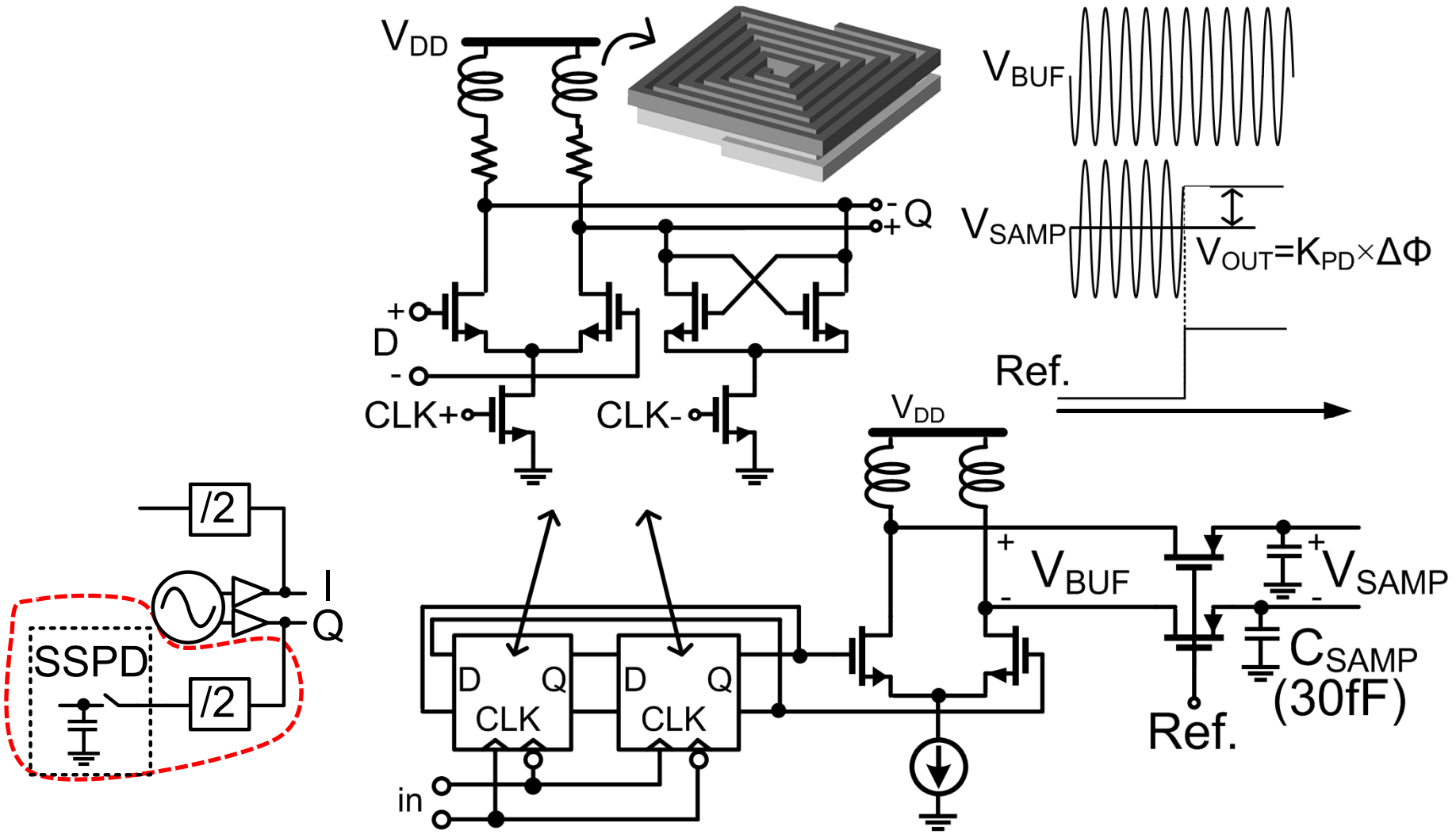
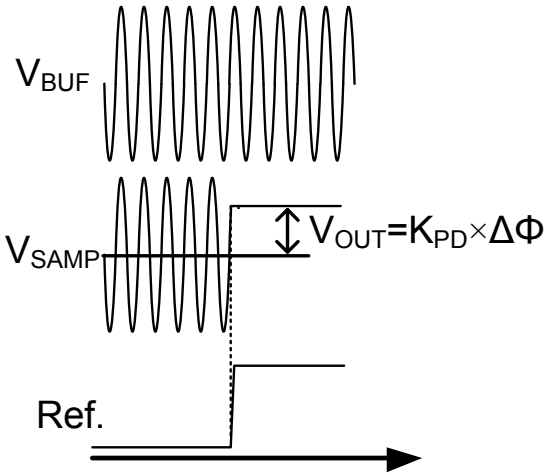
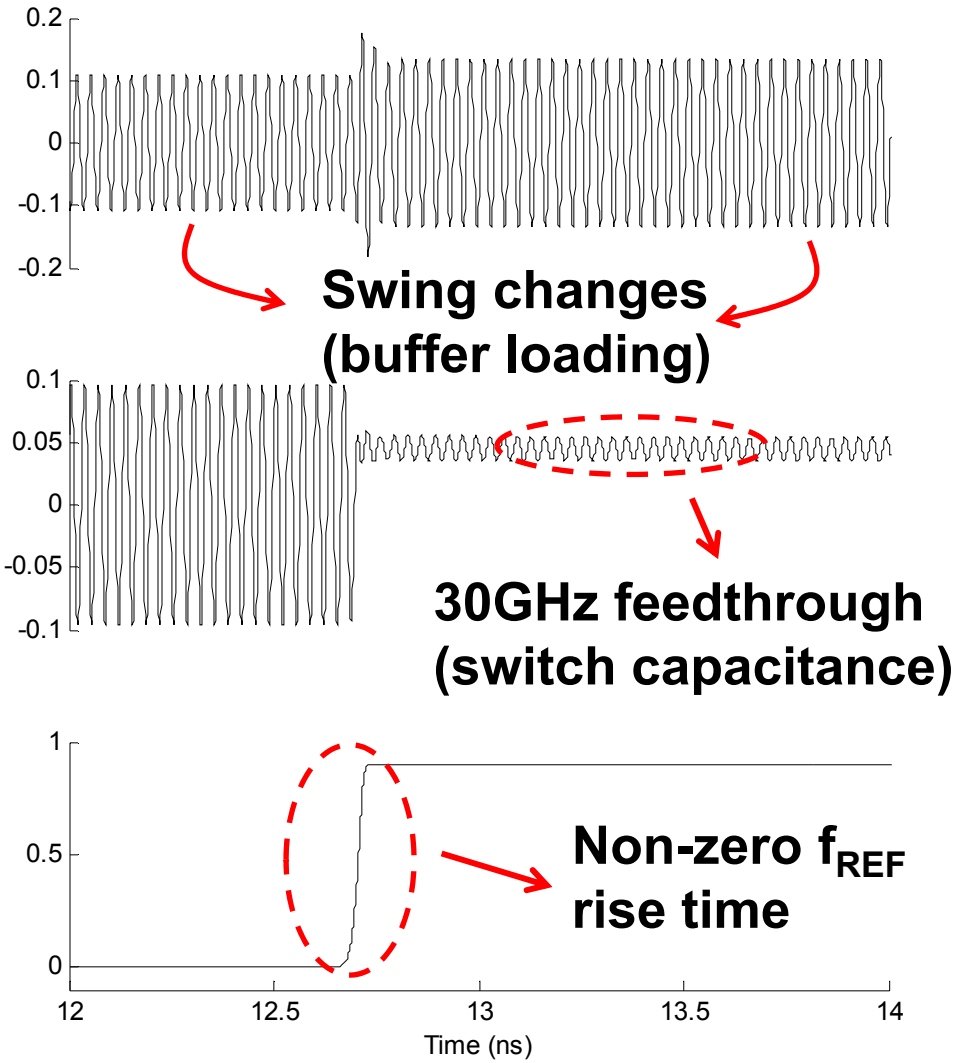
Divider+SSPD



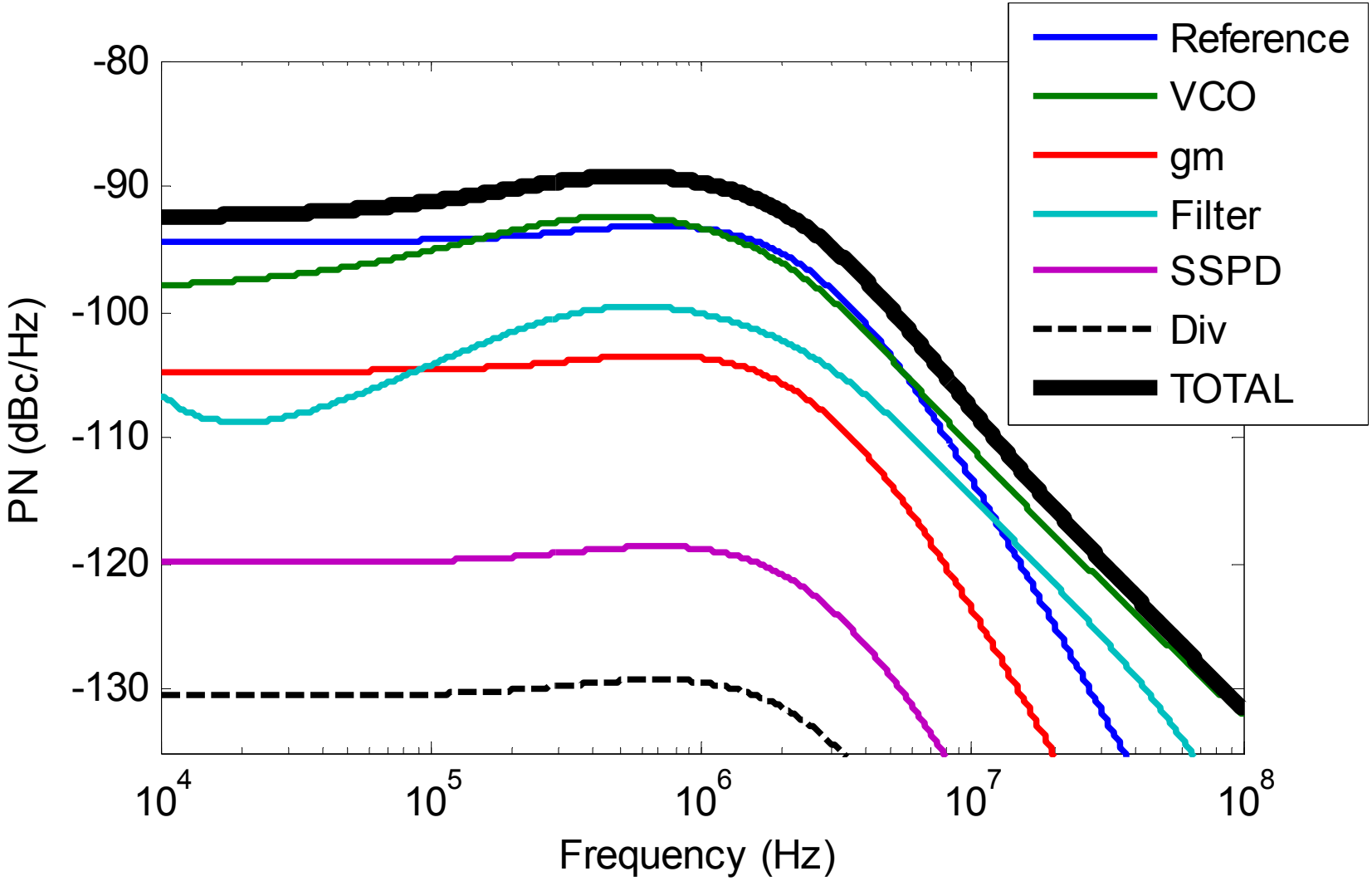
Simulated SSPD at 30GHz

Ideally:





SSPLL noise modeling



Outline

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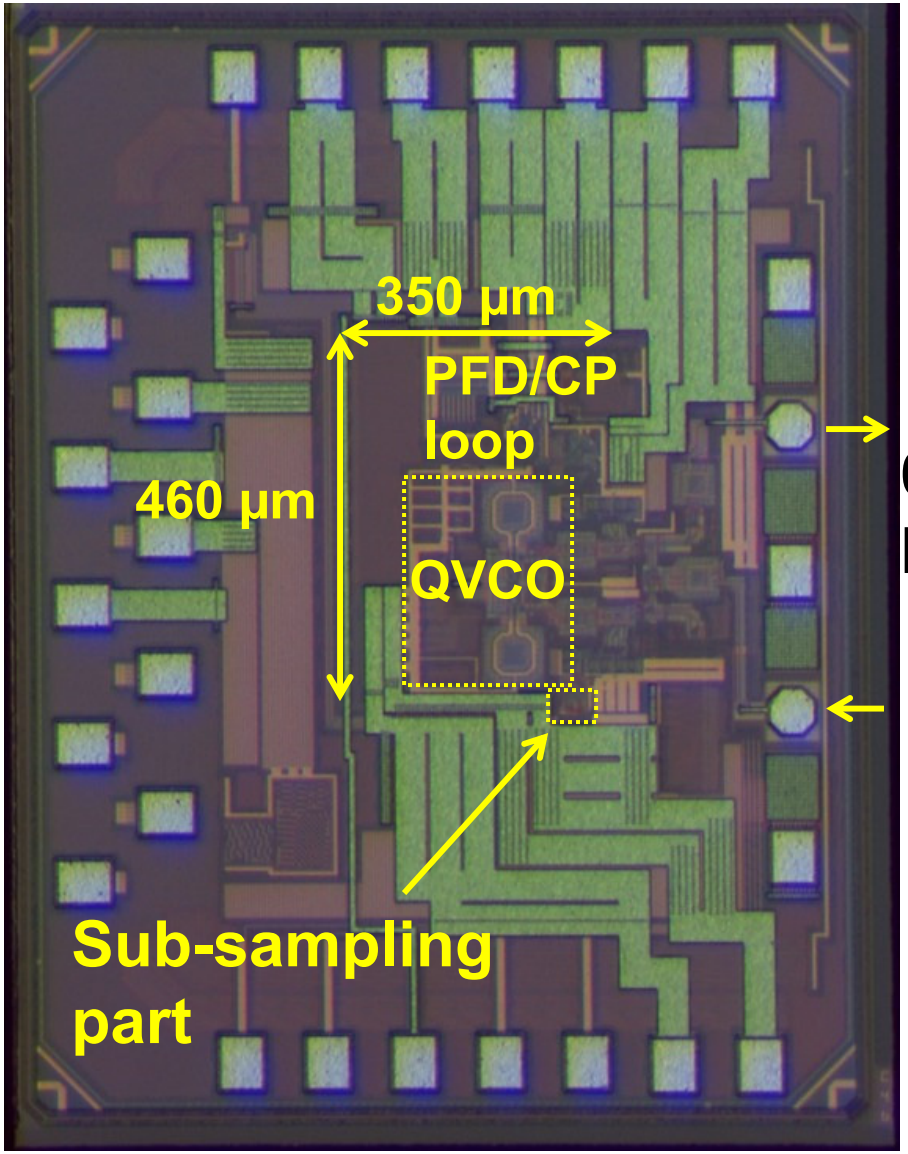
- Summary

Test chip

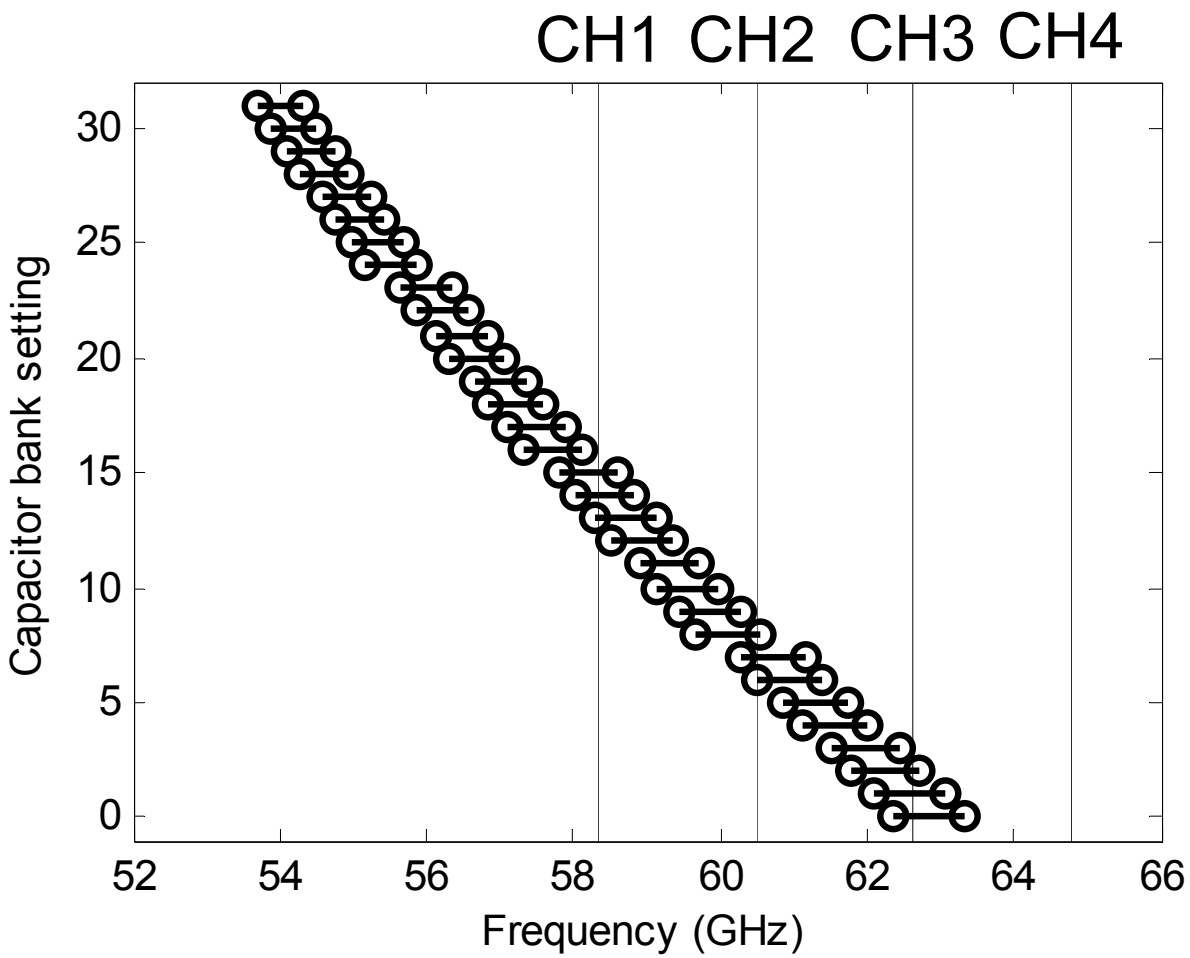


- 40nm GP CMOS
- Core area 350x460µm²
- V_{DD}=0.9V/1V
- 42mW SSPLL

60 GHz PLL out

60 GHz LO in

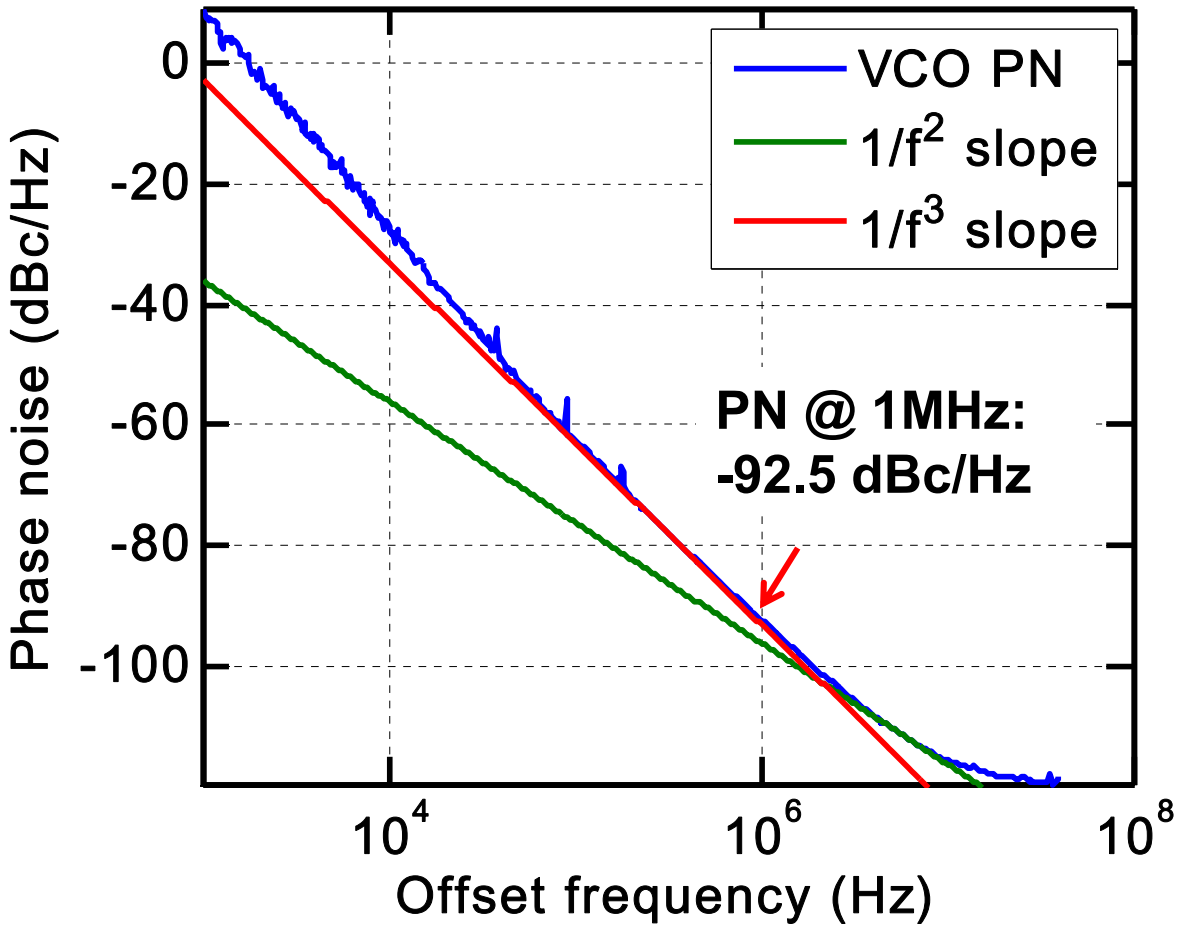
QVCO measurement: tuning range



Tuning range:

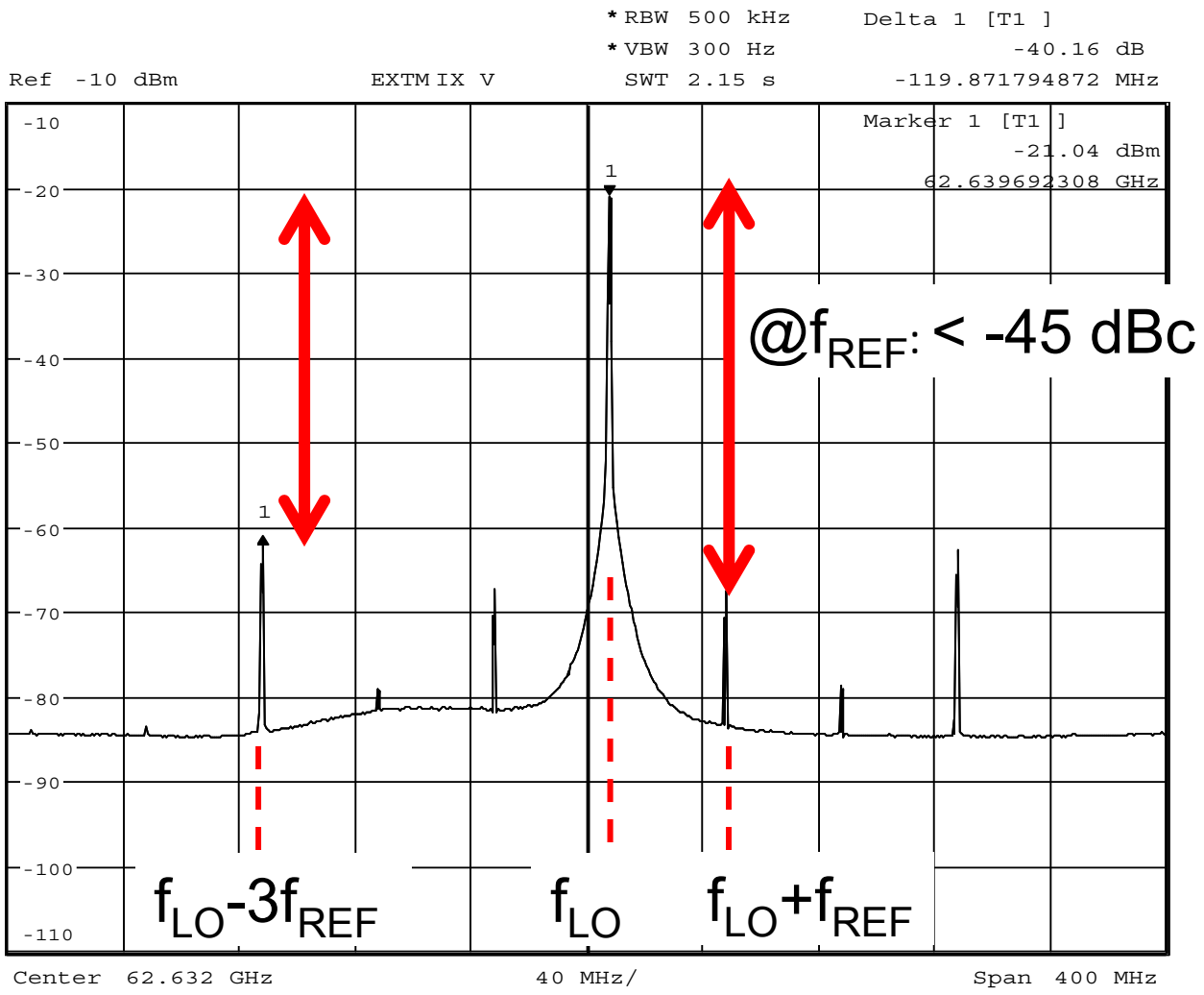
- 9.5 GHz (16.2%)
- 53.8-63.3 GHz

QVCO measurement: phase noise

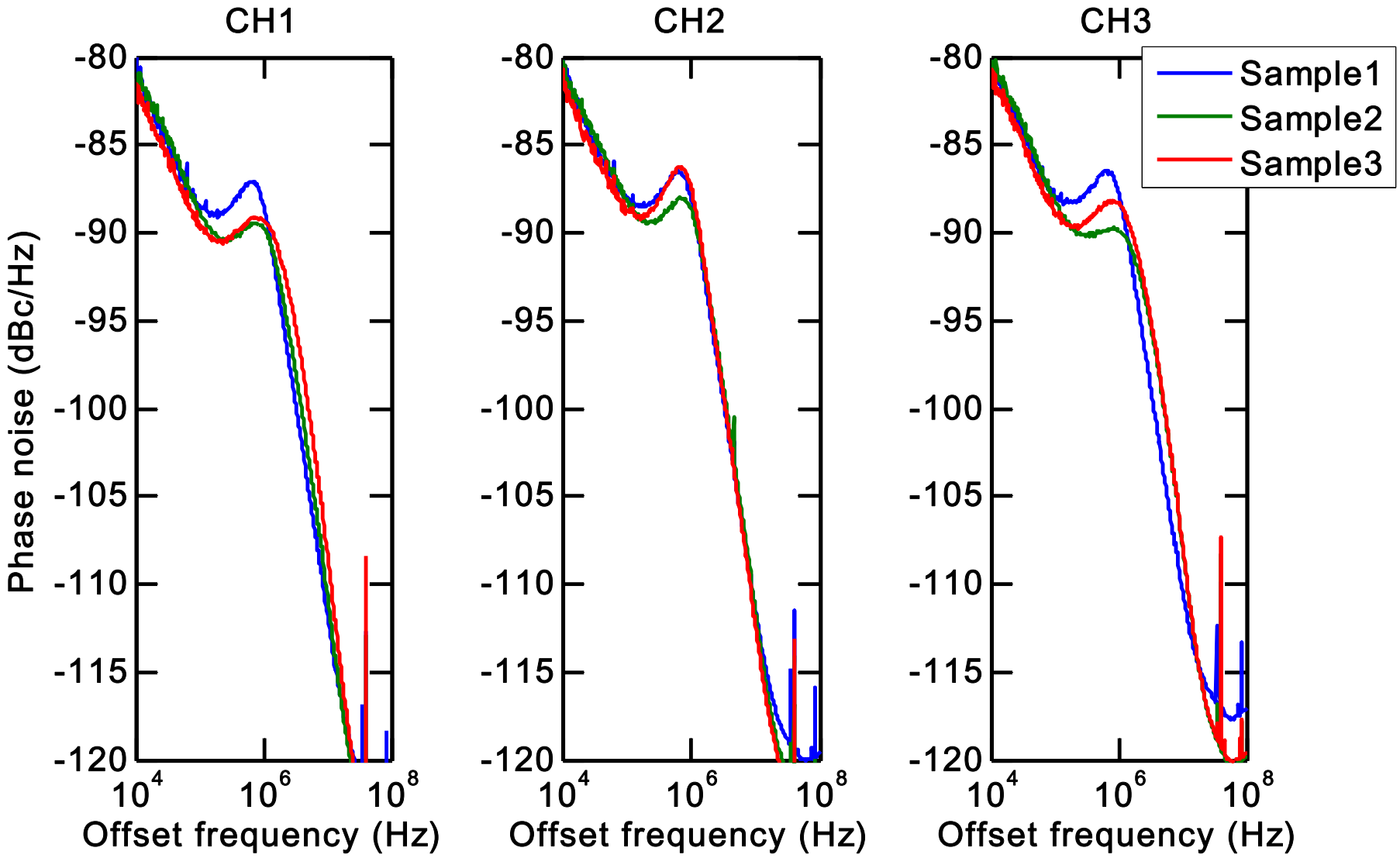


SSPLL output spectrum

-40.16dBc worst-case spur @$3f_{REF}$

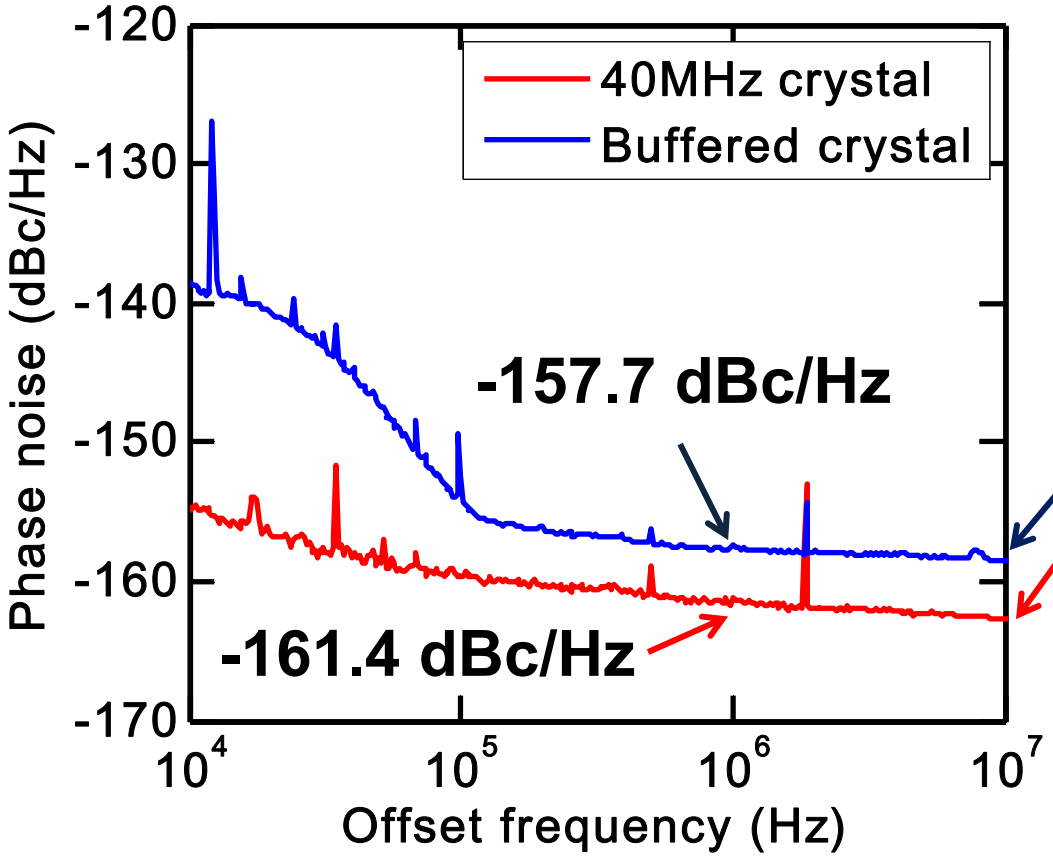


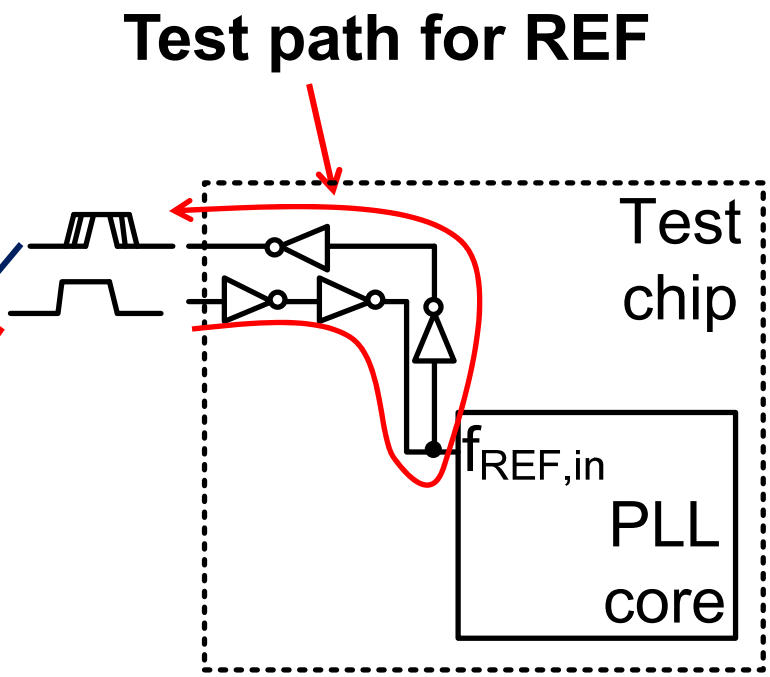
SSPLL: measured phase noise



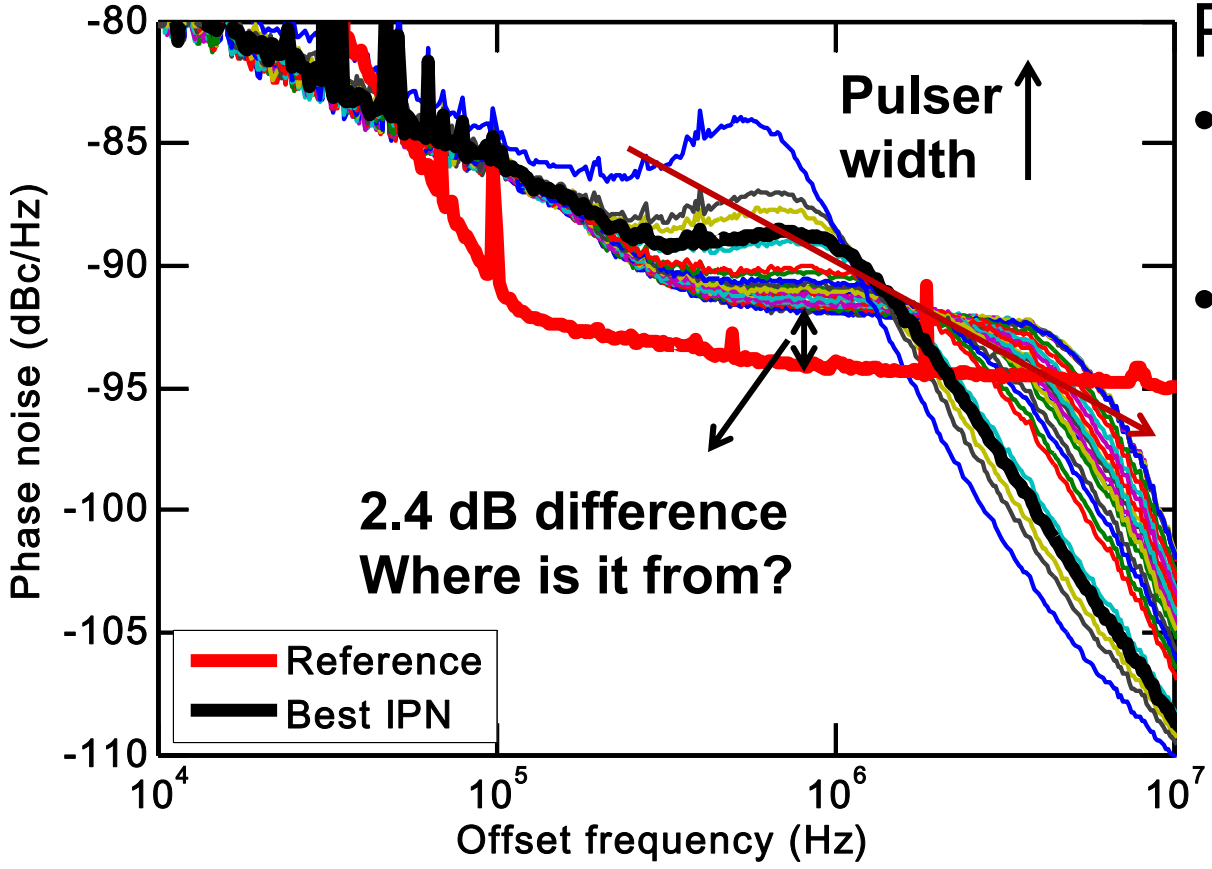
Reference phase noise

- Almost 4dB degradation
- Ref. t_{RISE}≈0.5-1ns
- Input stage dominates added PN





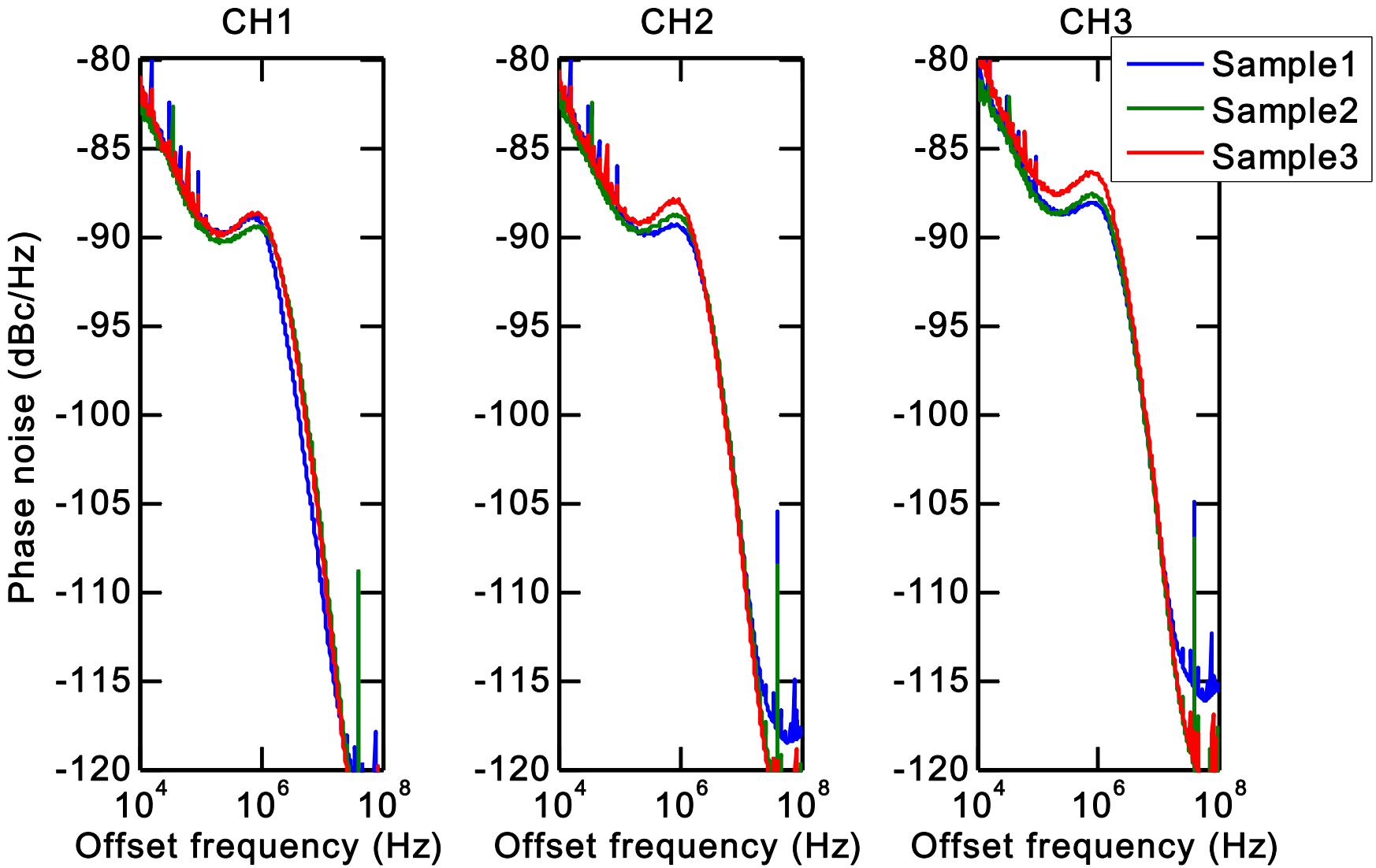
In-band phase noise: where is the limitation?



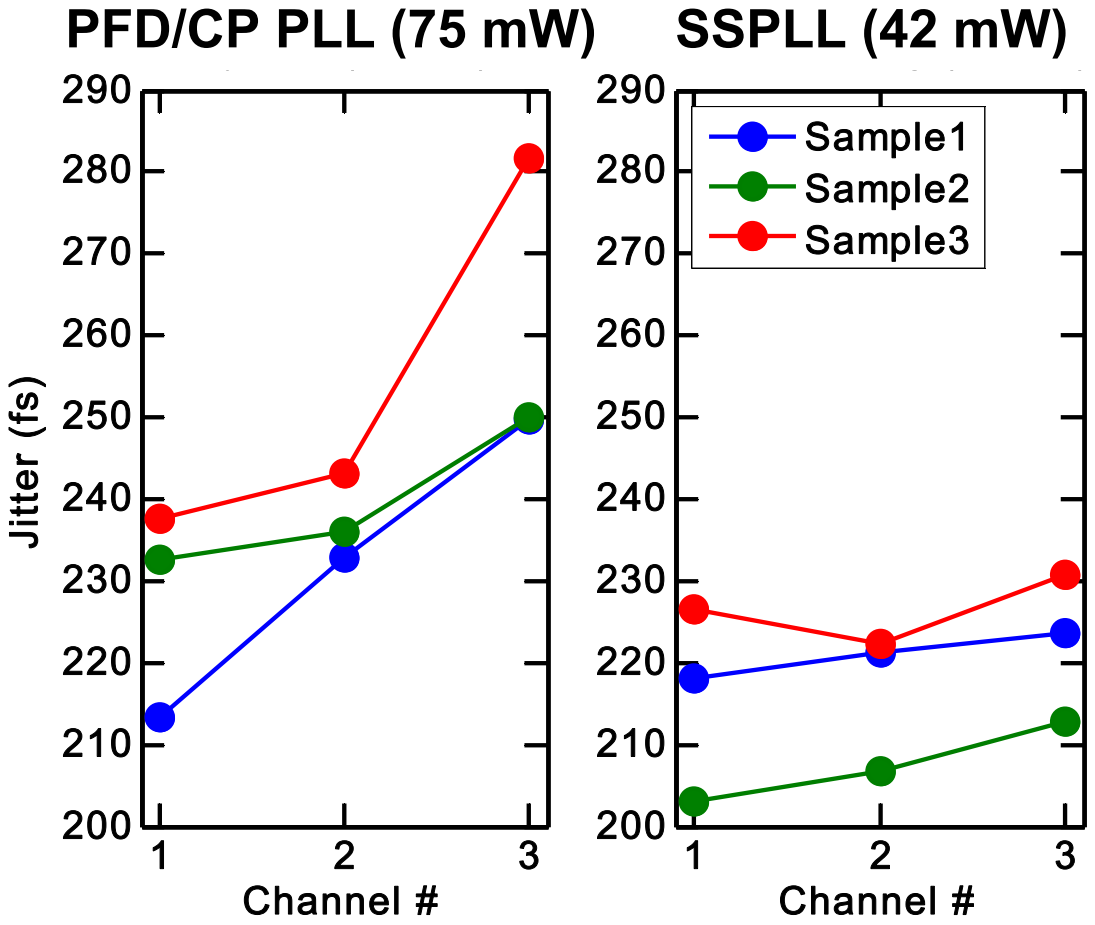
Possible reasons:

- Jitter in f_{REF} distribution
- Decreased swing at SSPD

PFD/CP PLL: measured PN

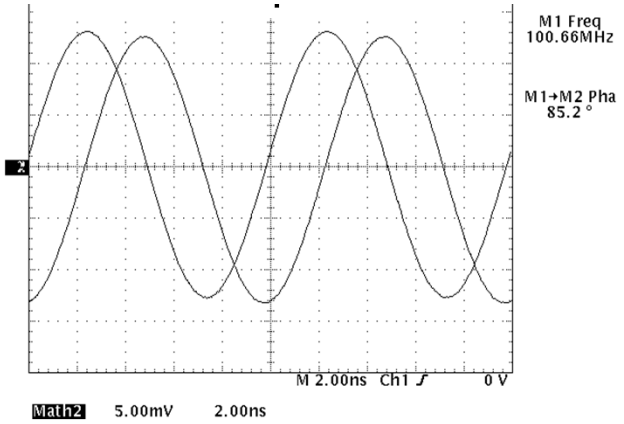


Jitter measurement and comparison

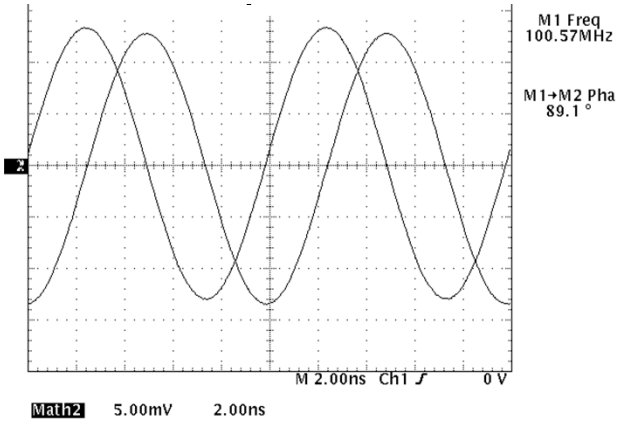


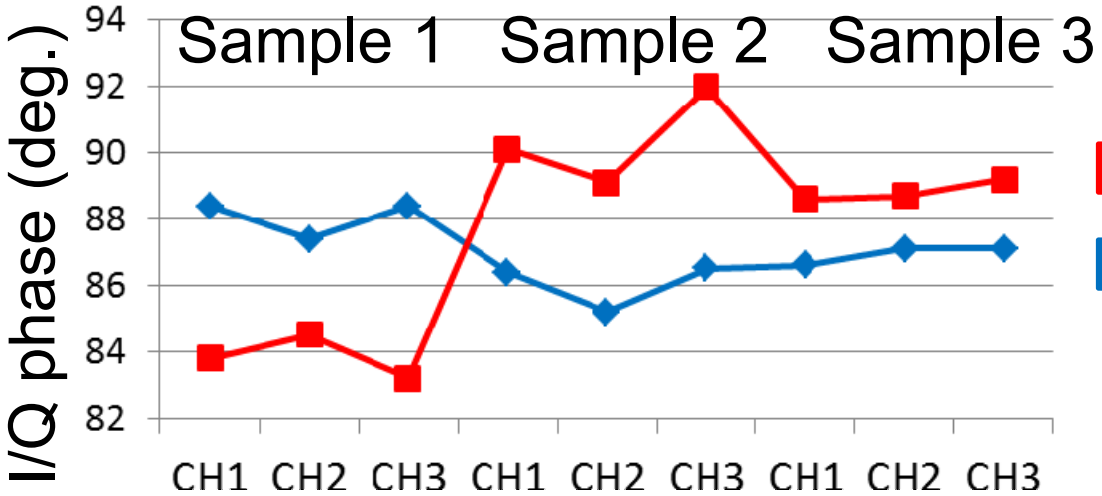
I/Q phase compensation

Before: 85.2 deg.



After: 89.1 deg.





After compensation

Before compensation

Performance summary

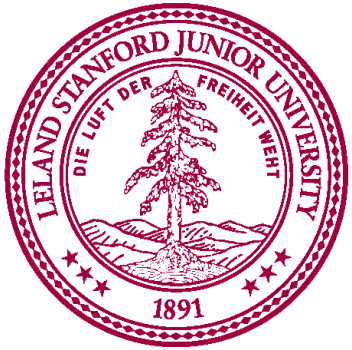
		This work		Yi ISSCC13	Wu ISSCC13	Murphy JSSC11	Deng JSSC13
Topology		**60GHz Subsampling QPLL**	**60GHz PFD/CP QPLL**	60GHz PFD/CP QPLL	60GHz ADPLL	50GHz PFD/CP PLL	20GHz PLL + 60GHz QILO
Type		**Integer-N**	**Integer-N**	Integer-N	Fractional-N	Integer-N	Integer-N
CMOS technology		**40nm**	**40nm**	65nm	65nm	65nm	65nm
Tuning range (GHz)		**53.8-63.3 (16.2%)**	**53.8-63.3 (16.2%)**	57.9-68.3 (16.5%)	56.4-63.4 (11.7%)	42.1-53 (22.9%)	58.1-65 (11.2%)
f_{REF} (MHz)		**40**	**40**	135	10 .. 100	54	24
Normalized phase noise (dBc/Hz)	In-band	**-89.6**	**-86.4**	N/A	-72	-81	N/A
	@1MHz	**-88.3**	**-89.7**	-91	-90	-95.56	-96
RMS jitter (fs)		**203-230**	**213-282**	238[c]	522.9	N/A	N/A
Area (mm^2)		**0.16**	**0.16**	0.19	0.48	0.37	3.8
P_{DC} (mW)	VCO (quadrature?)	**30 (yes)**	**30 (yes)**	11.4 (yes)	13.2 (no)	N/A (no)	N/A (yes)
	Loop components	**12**	**45**	13.2	34.8	N/A	N/A
	Total	**42**	**75**	24.6[b]	48[b]	72	72

Conclusion

- Sub-sampling PLL at mm-Wave frequencies
  - Lower jitter (230fs) and P_{DC} (42mW)
  - Sampler in the dummy divider
- 60 GHz QVCO
  - Superharmonic coupling at 120 GHz
  - Fully automatic phase calibration

A 3.24-to-8.45GHz Low-Phase-Noise Mode-Switching Oscillator

Mazhareddin Taghivand, Kamal Aggarwal and Ada Poon



Dept. of Electrical Engineering
Stanford University

Outline

- **Motivation**
- **Design Challenges**
- **Design of Mode-Switching VCO**
- **Measurement Results**
- **Conclusion**

Motivation

- **Cellular/WiFi frequencies from 400-to-5900MHz**
- **Multiple VCOs are used for multi-band**
  - x **Area increases**
  - x **Muxing of VCO outputs**
- **Need to meet stringent PN requirements**
  - **One-turn inductor is needed → large area**
  - **Coupling multiple VCOs → high power & area**

Motivation

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  - x **Area increases**
  - x **Muxing of VCO outputs**
- **Need to meet stringent PN requirements**
  - **One-turn inductor is needed → large area**
  - **Coupling multiple VCOs → high power & area**
- **Desirable to have one VCO with**
  - ✓ **Low PN**
  - ✓ **Wide tuning range**

Outline

- Motivation
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Low PN VCO Design

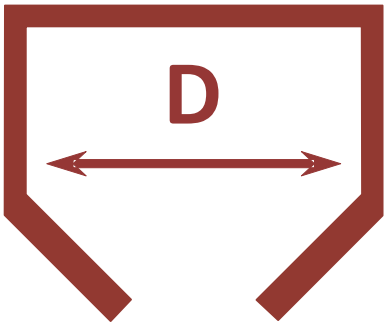
- **Best PN from Leeson's eq.**
  - **Maximize voltage swing → reliability limit**
  - **Maximize Q of the LC tank**
  - **Increase Capacitance → Reduce Inductance**

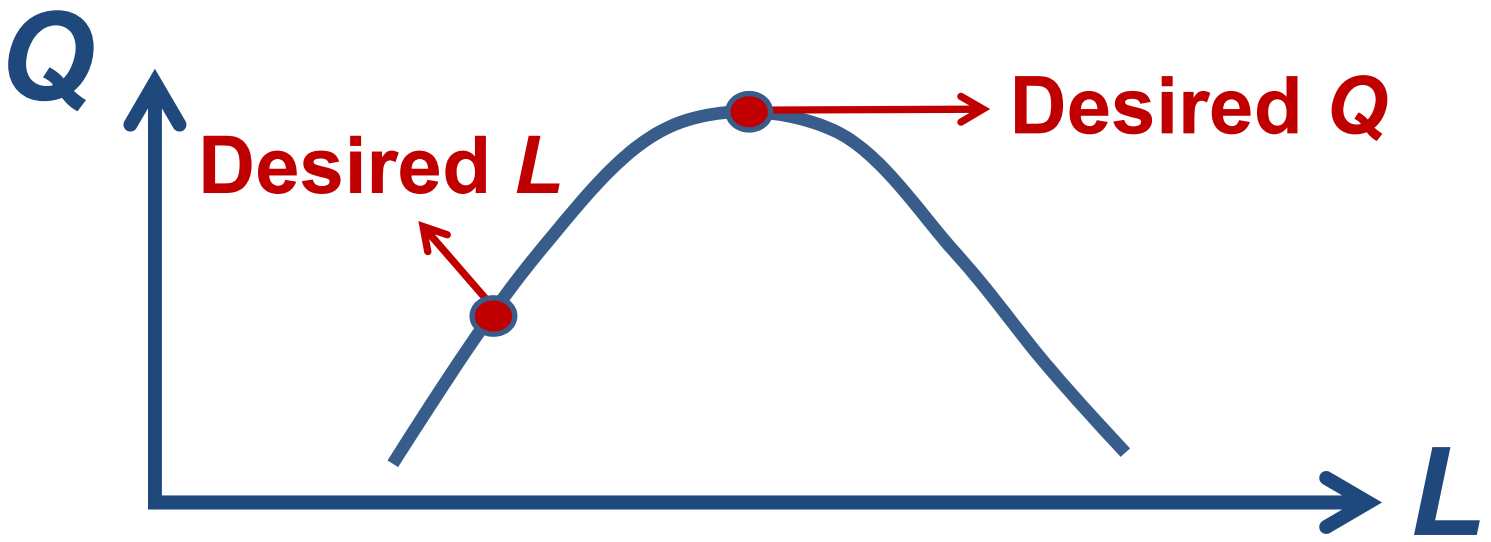
$$PN\downarrow \propto \left(\frac{KT}{C\uparrow}\right)\left(\frac{1}{Q\uparrow V^{2}\uparrow}\right)$$

Small Inductance Challenge

- **Inductance & Q increase with area**

$$Q = \frac{L\omega}{R} \propto \frac{D^2\omega}{D} \propto D\omega$$





Outline

- Motivation
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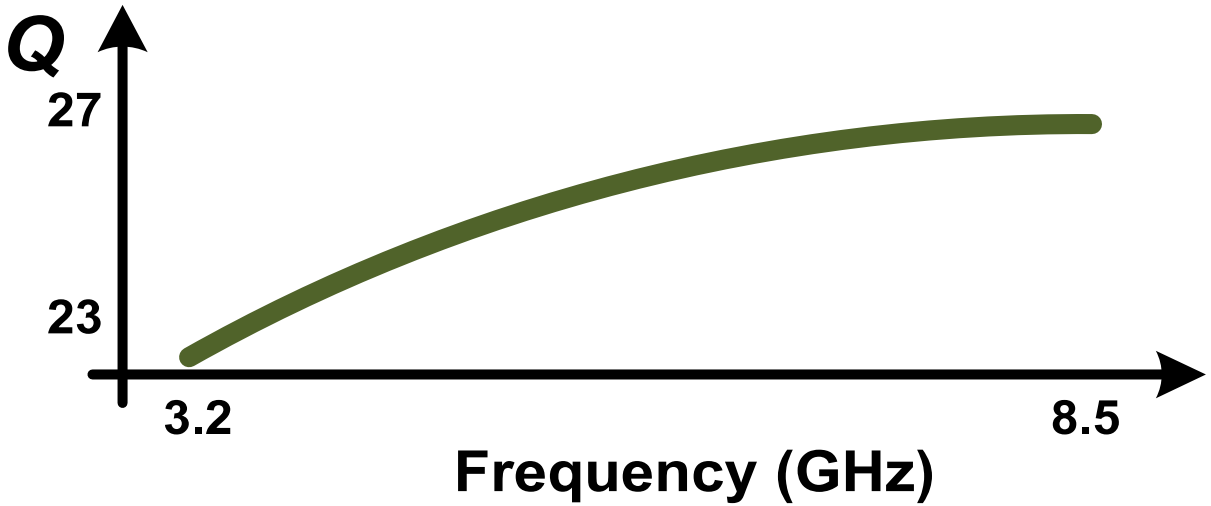
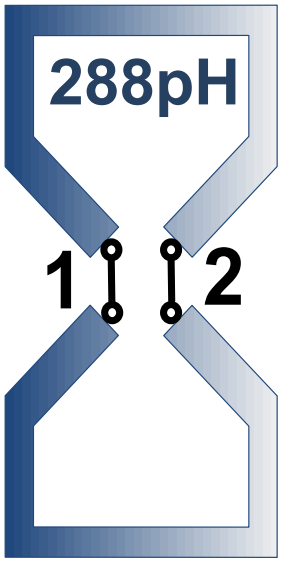
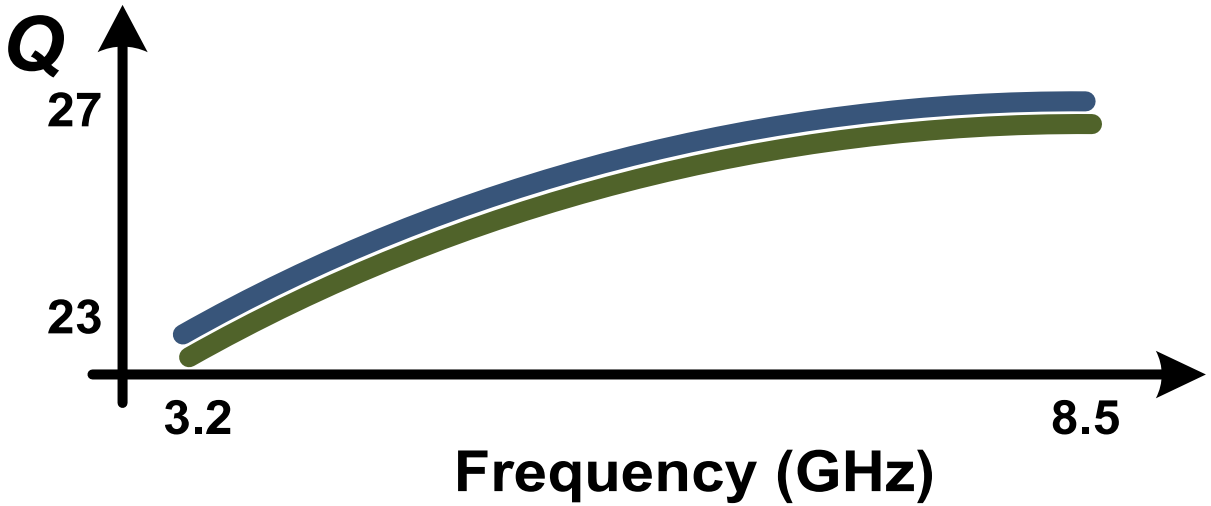
High Q & Small Inductance

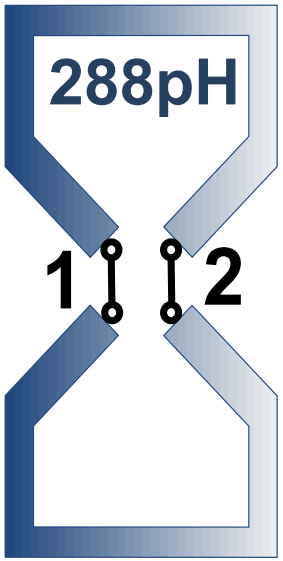


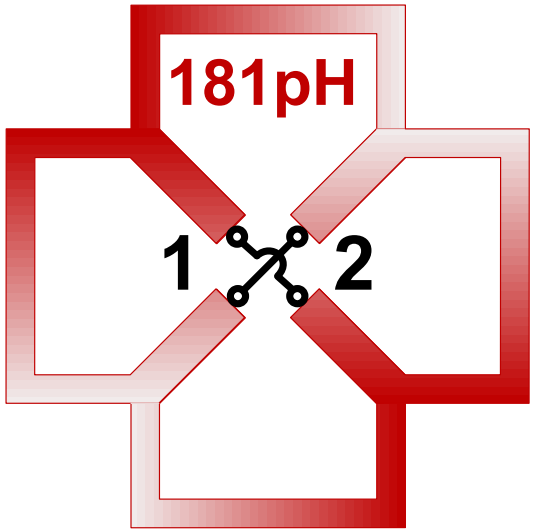
High Q & Small Inductance

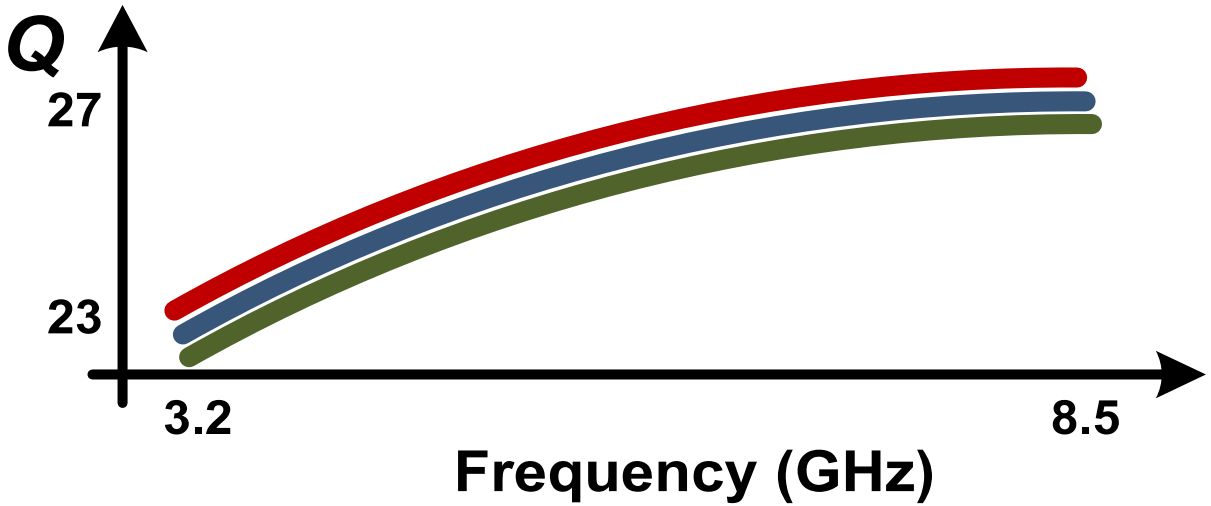




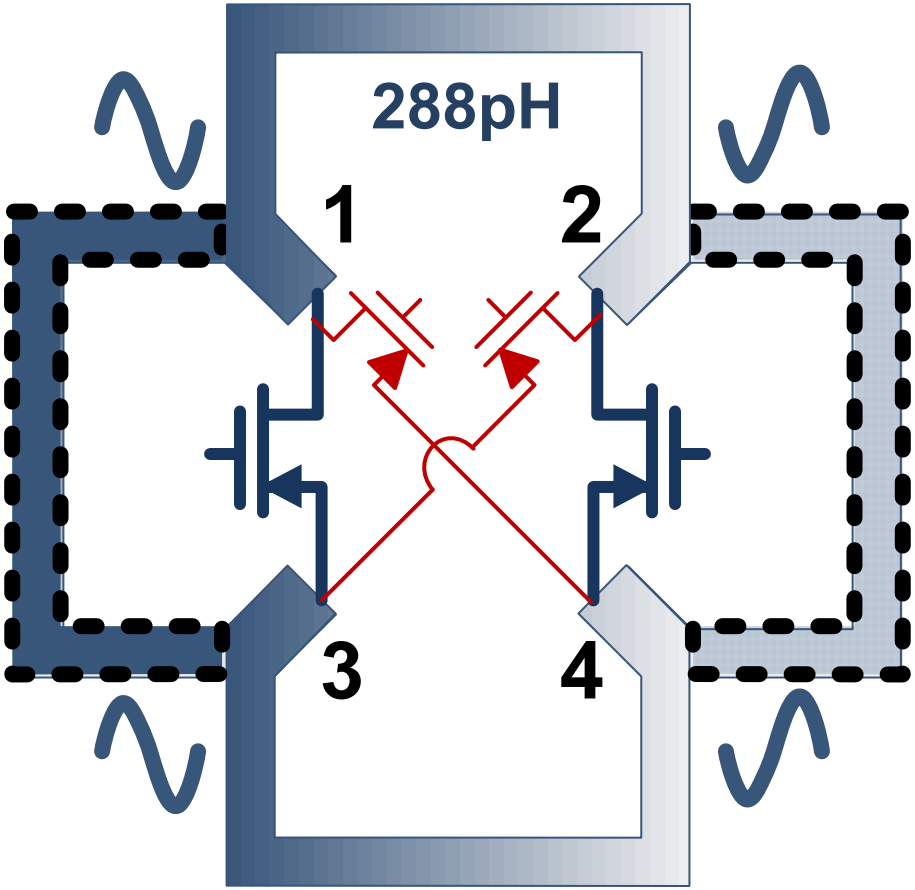
High Q & Small Inductance







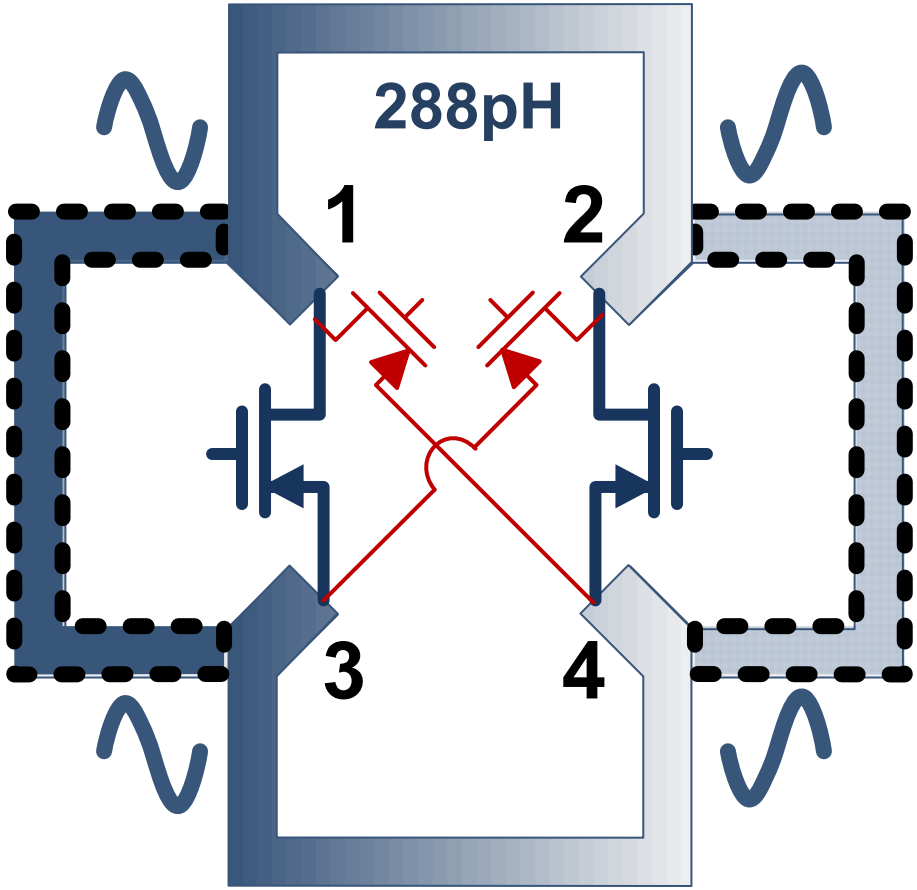
Mode Switching Inductor



Common mode voltage

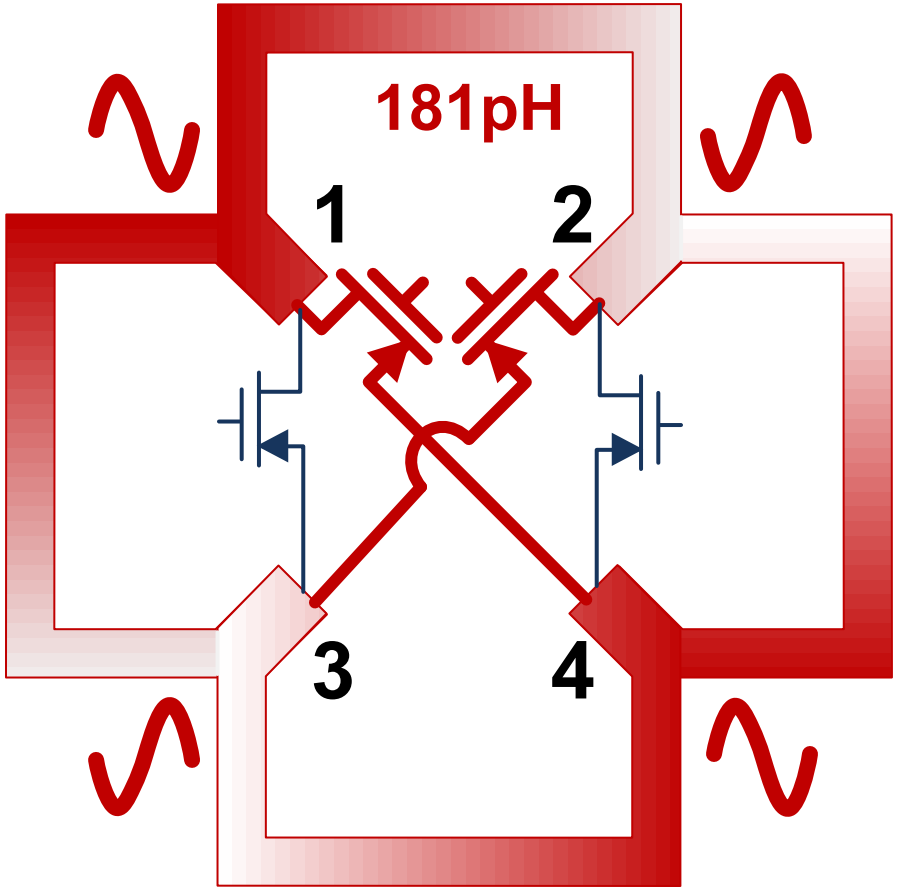
No loss in switches

Mode Switching Inductor



Common mode voltage

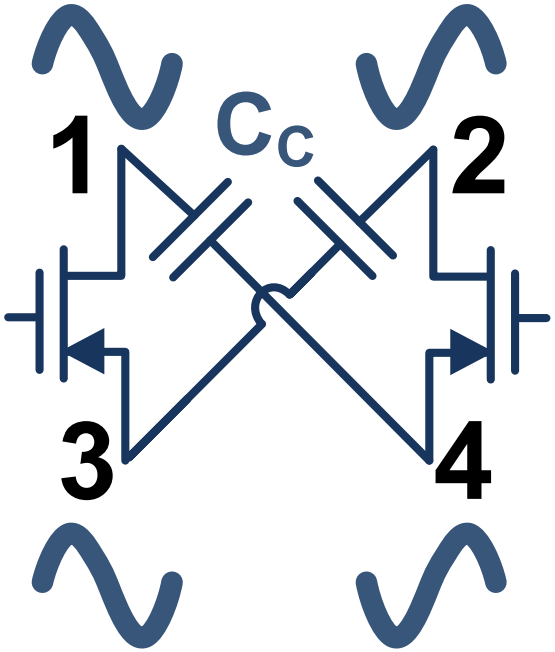
No loss in switches

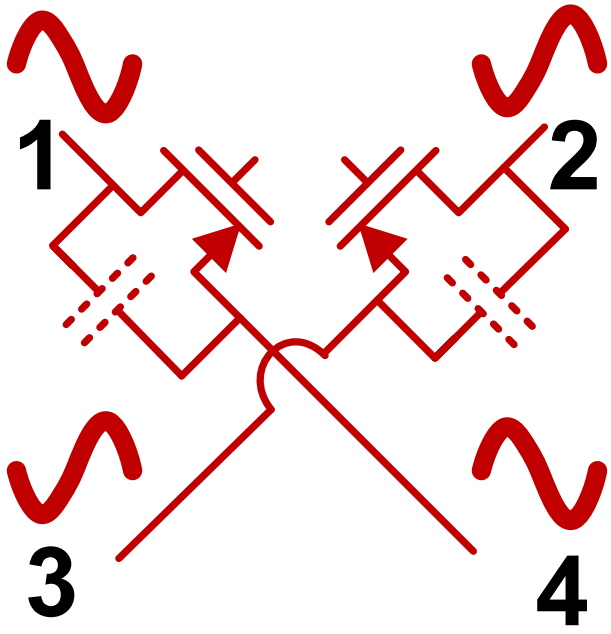


Common mode voltage

No loss in switches

Mode Switching Capacitor

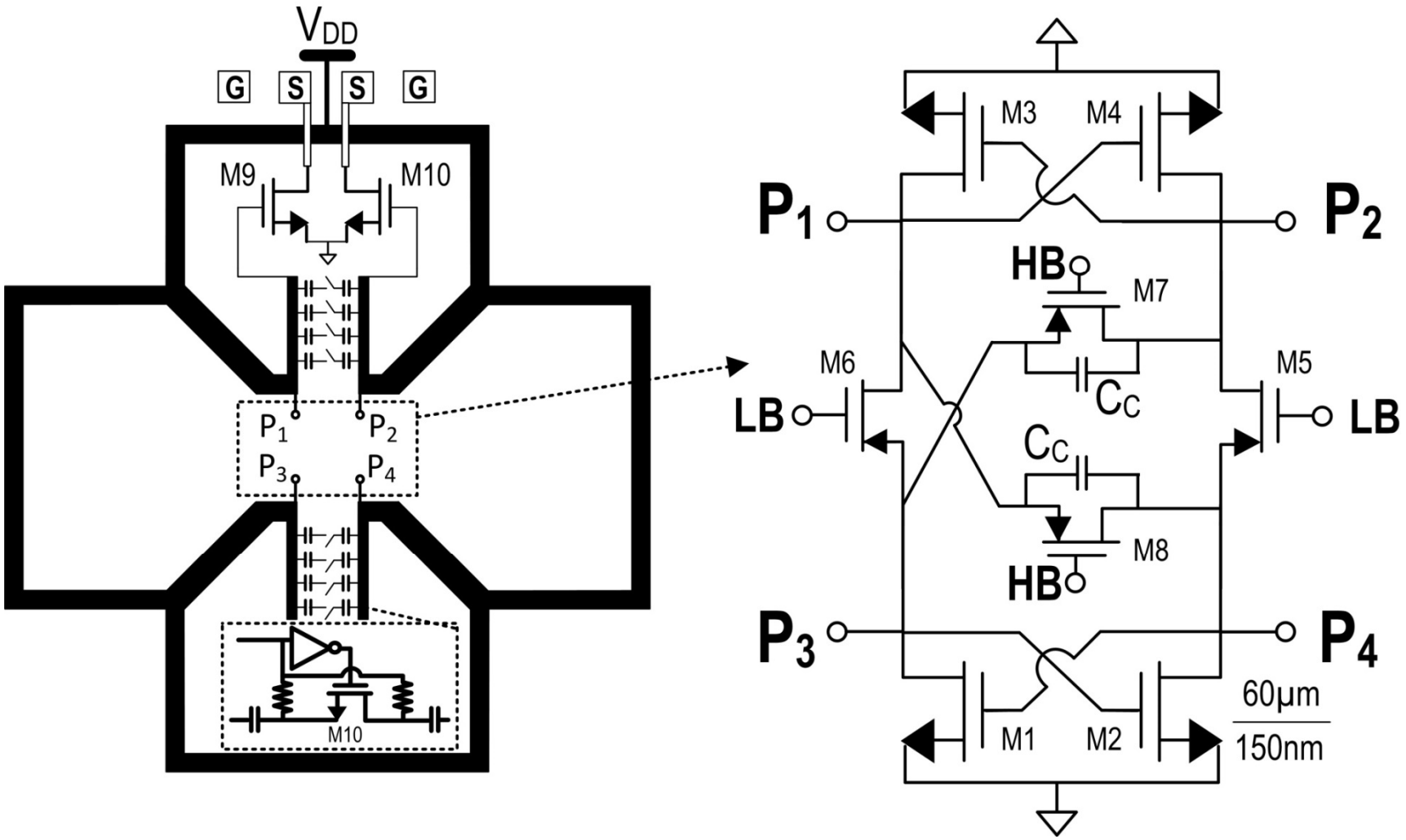




$$\omega = \frac{1}{\sqrt{L_{High}\left(C + C_C\right)}}$$

$$\omega = \frac{1}{\sqrt{L_{Low} C}}$$

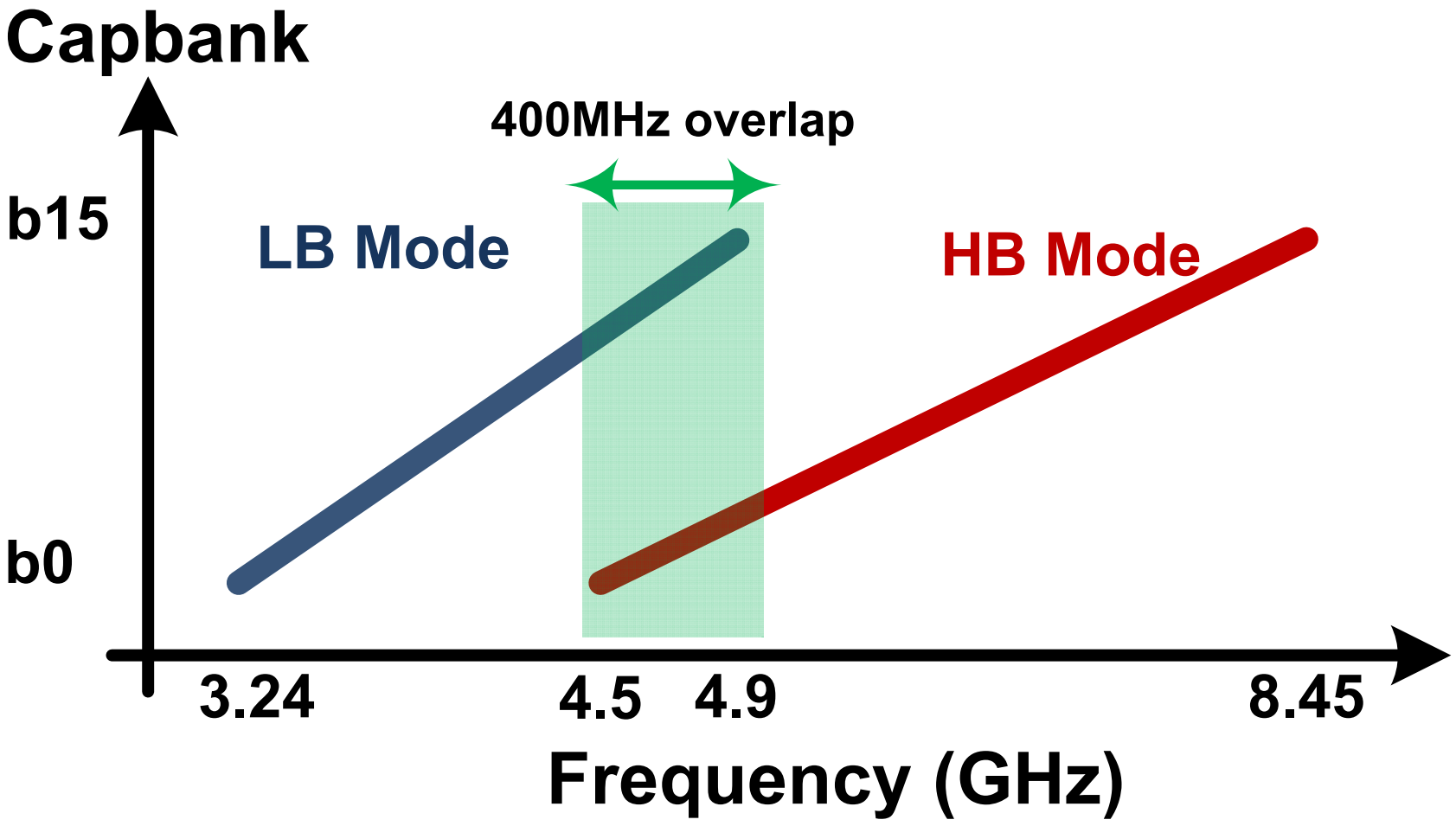
Mode Switching VCO



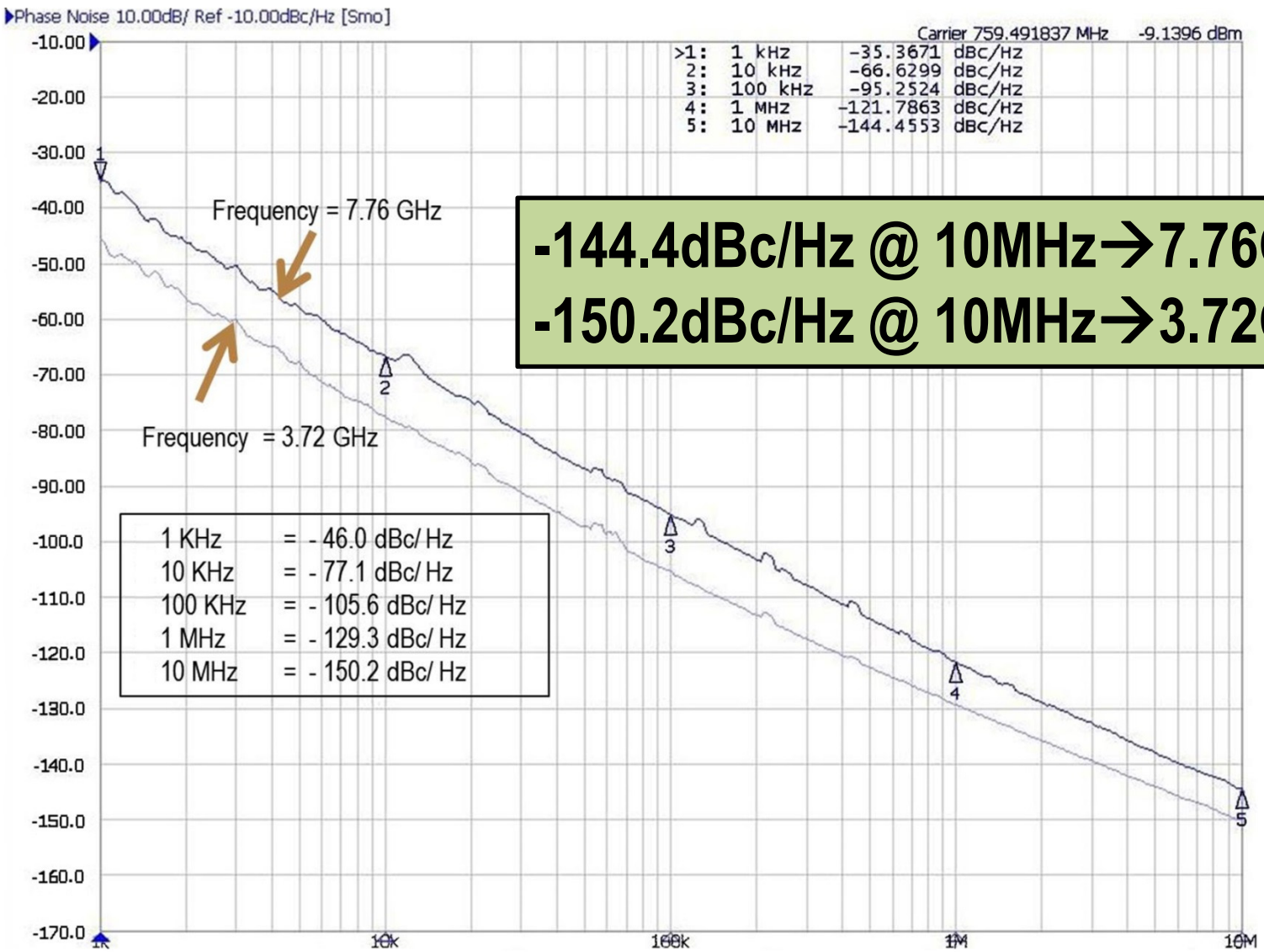
Outline

- Motivation
- Design Challenges
- Design of Mode-Switching VCO
- Measurement Results
- Conclusion

Frequency Range



Measured Phase Noise



-144.4dBc/Hz @ 10MHz→7.76GHz

-150.2dBc/Hz @ 10MHz→3.72GHz

Measured PN @ 0.8V

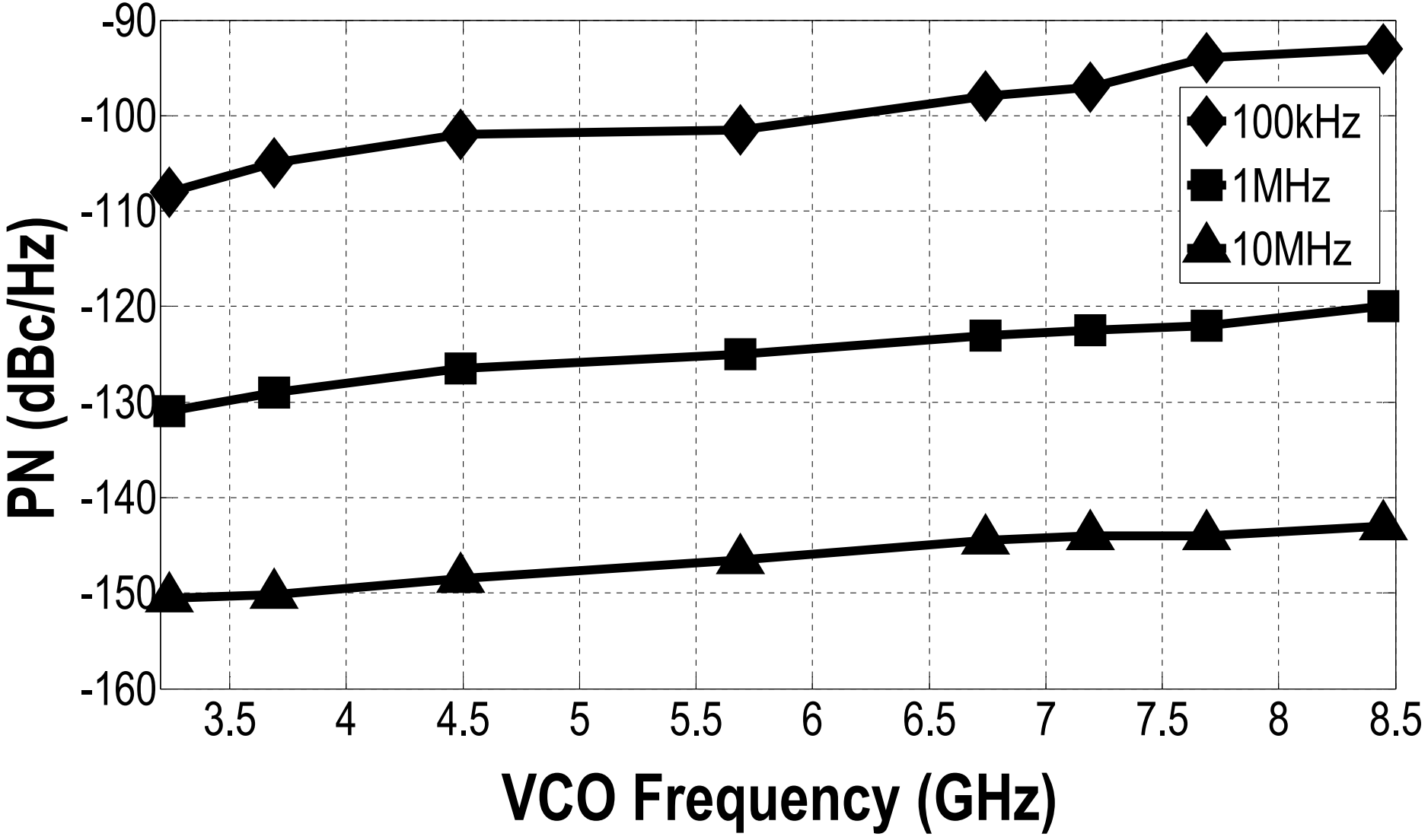
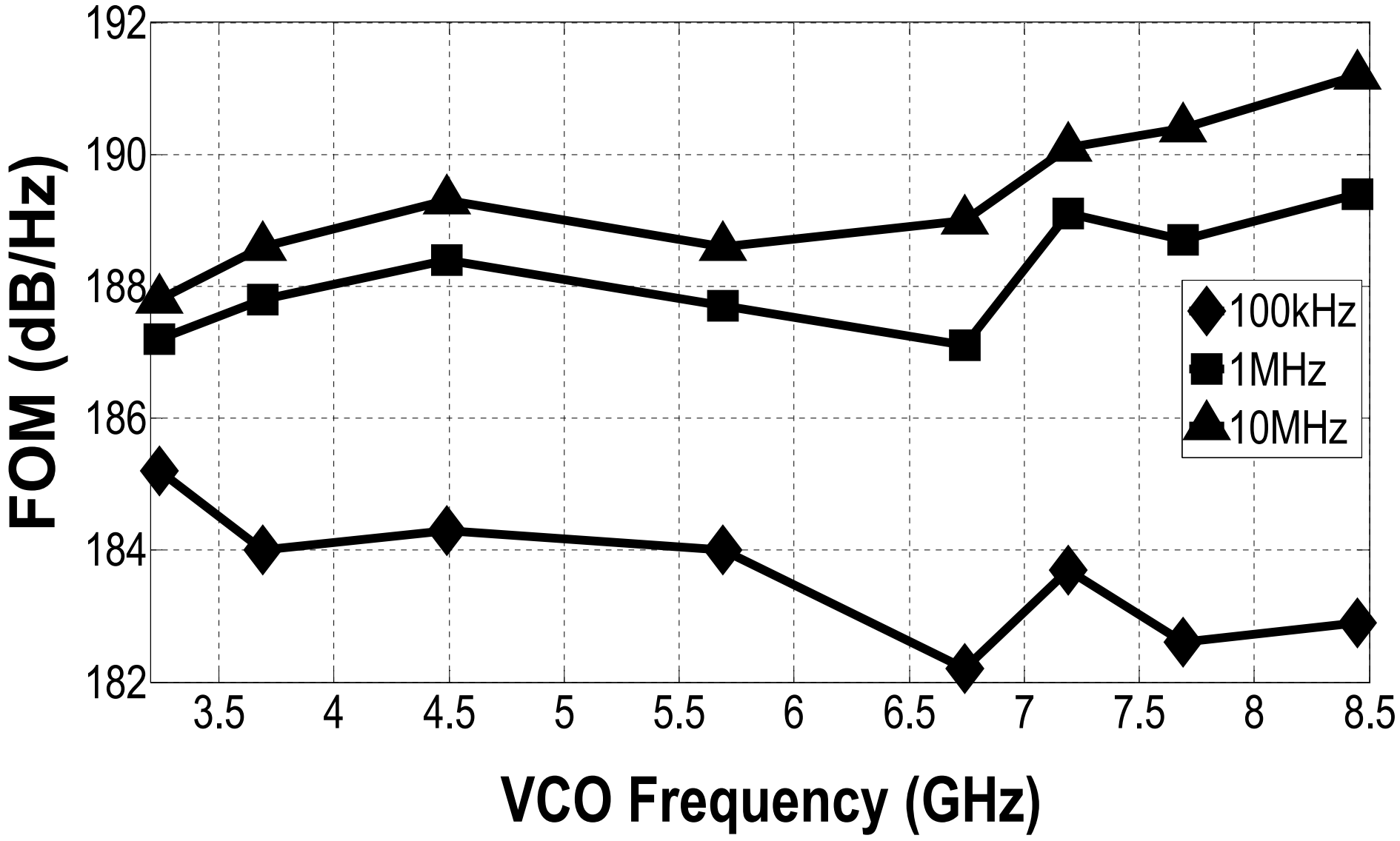
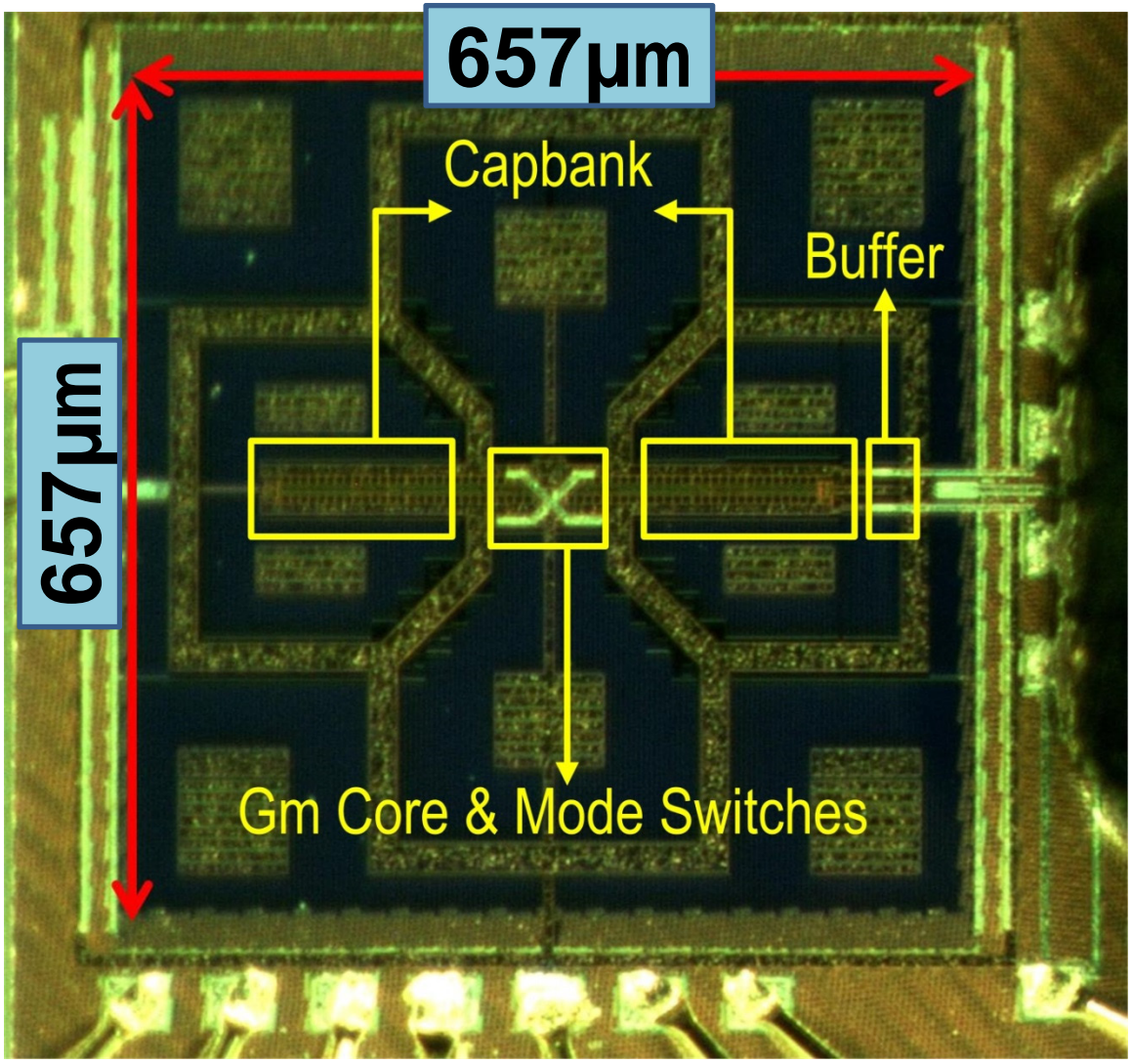


Figure of Merit



Die Photo



Outline

- Motivation
- Design Challenges
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Table of Comparison

	This Work		ISSCC. 2012	JSSCC June 2012	CICC 2009
Frequency (GHz)	3.24 – 8.45 (88.7 %)		6.72 – 9.2 (31%)	2.48 – 5.62 (77.5%)	3.28-8.35 (87.2%)
Core Voltage (V)	0.8		1.5	0.6	1.6
Core Power (mW)	20		27	9.8 - 14.2	6.5 - 15.4
Carrier (GHz)	3.72	7.76	3.72*	3.72*	3.72*
PN (dBc/Hz) @ 100 KHz offset	-105.56	-95.25	-104	-96	-95
FoMT(dB/Hz) @ 100 KHz offset	202.92	199.05	191	195	197
PN (dBc/Hz) @ 10 MHz offset	-150.22	-144.45	-151	-151.4	-141
FoMT(dB/Hz) @ 10MHz offset	207.58	208.25	198	210	203
Technology	40nm CMOS		55nm CMOS	65nmCMOS	130nm CMOS

Conclusions

- **Dual-band mode switching oscillator demonstrated**
- **Wide tuning range of 3.24GHz to 8.45GHz**
- **Low PN of −144.4dBc/Hz @ 10MHz offset of 7.76 GHz**
- **High FoMT of 208.2dB/Hz @ 10MHz offset for 7.76 GHz**

Acknowledgement

- TSMC University Shuttle Program
- Lorentz Solution for the EM tool
- Denny Goetz for help with testing

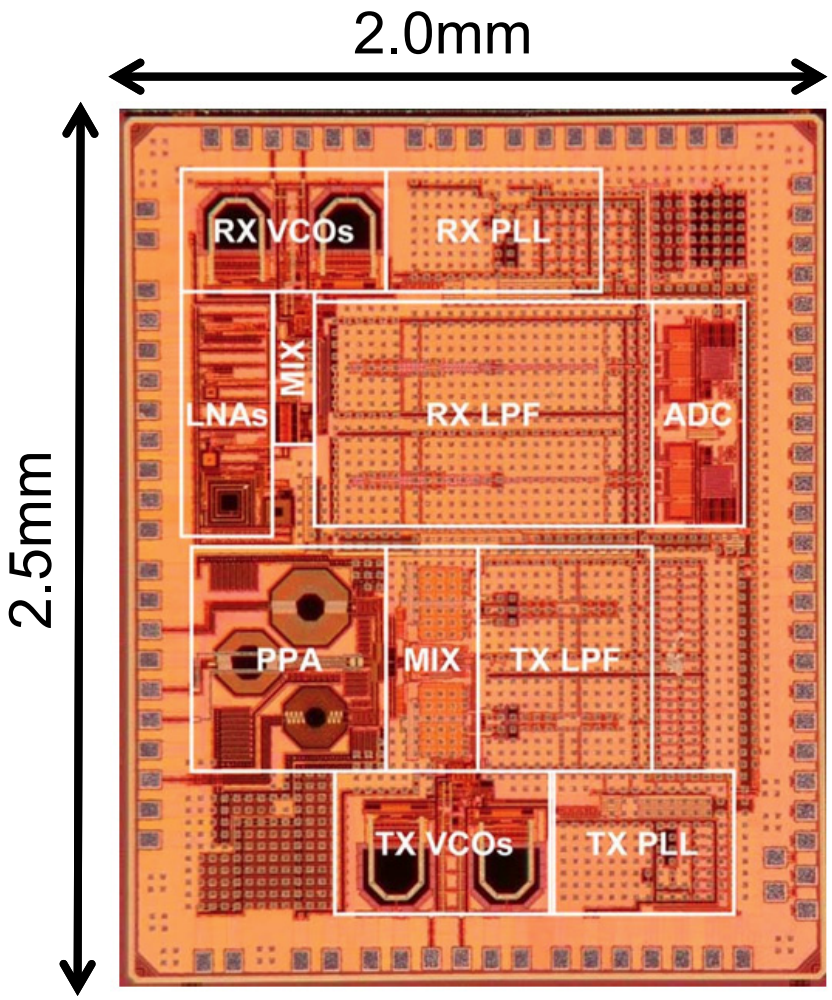
A 2.4-to-5.3GHz Dual-Core CMOS VCO with Concentric 8-Shaped Coils

Luca Fanori[1,2], Thomas Mattsson[3] and Pietro Andreani[1,3]

[1]Lund University, Sweden; [2] now with Marvell, Pavia, Italy;

[3]Ericsson Modems, Lund, Sweden

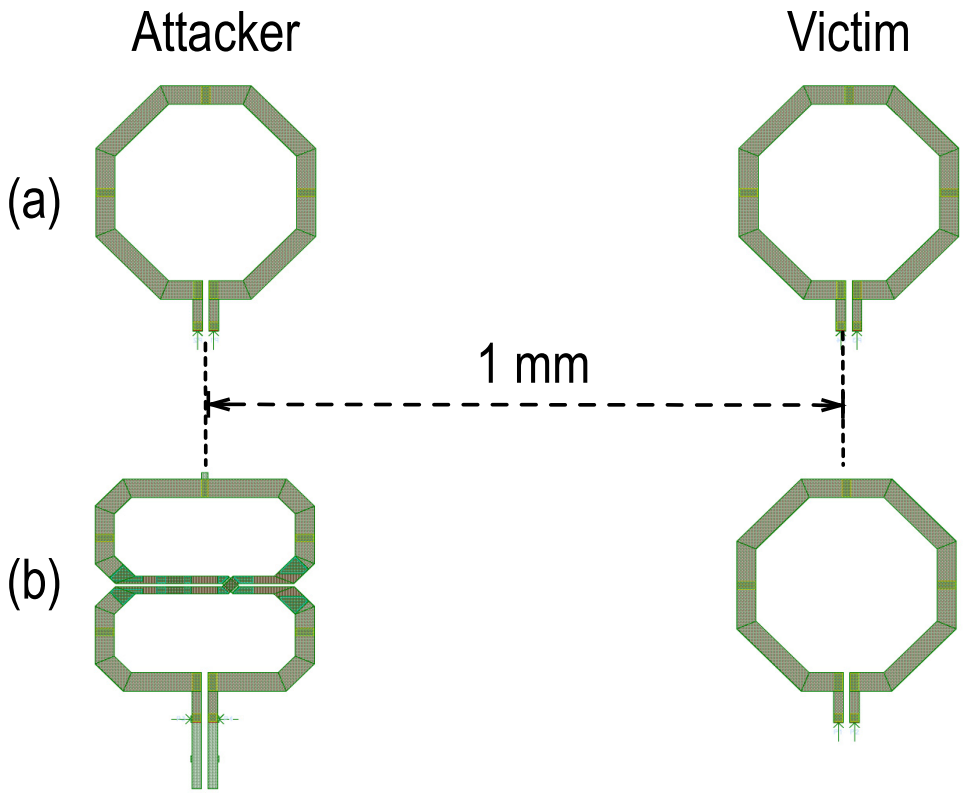
PLL area in LTE transceiver



- RX/TX PLLs occupy 30% area in single-carrier scenario
- RX/TX carrier aggregation duplicates PLL count
- High cost of nm CMOS imposes area awareness

Ingels et al., JSSC'10 – CMOS 40nm

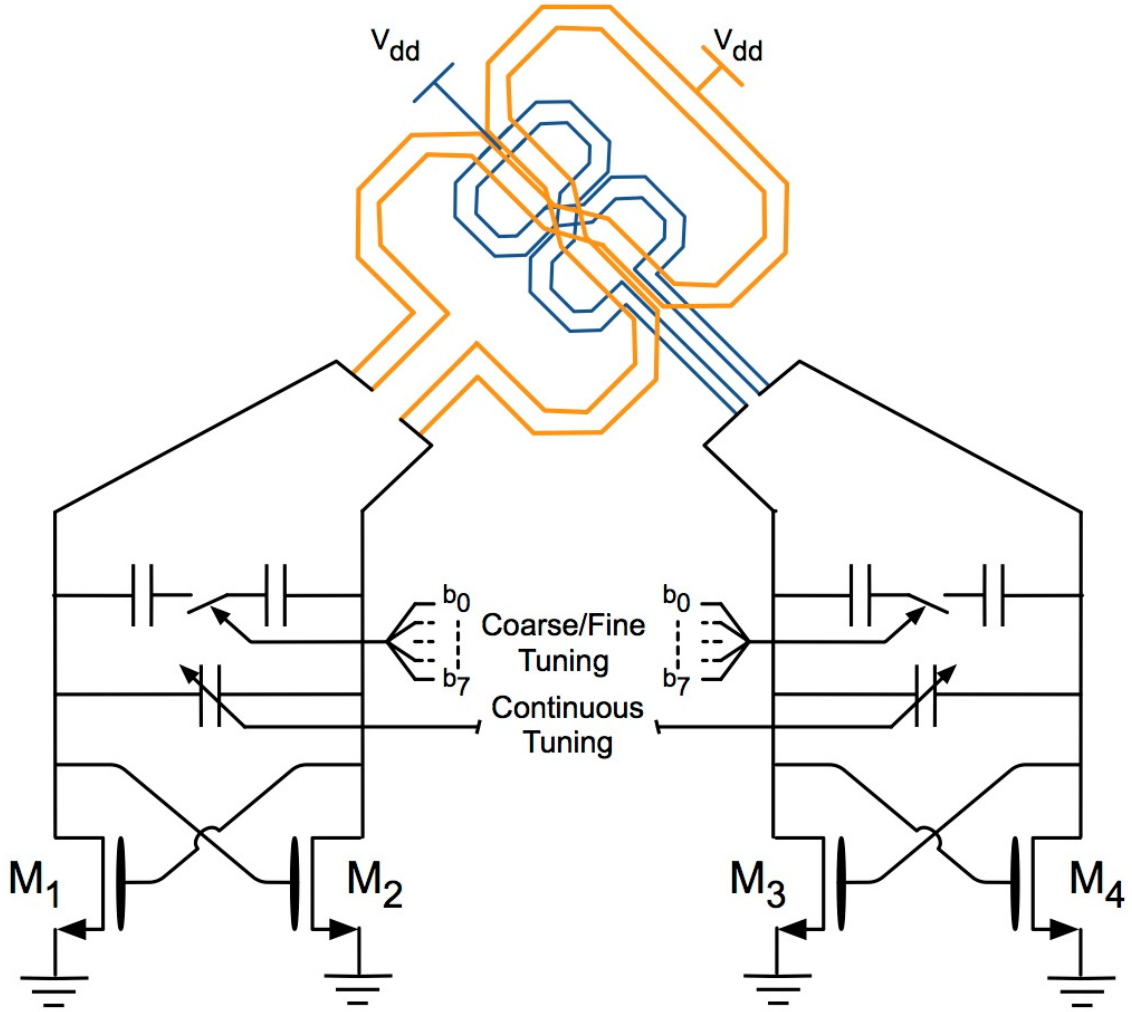
Mutual pulling between VCOs



	S_{21} at Victim
(a)	reference
(b)	**-39dB**

- 2 VCOs working simultaneously at close frequencies → critical pulling issue
- 8-shaped coils more immune to pulling

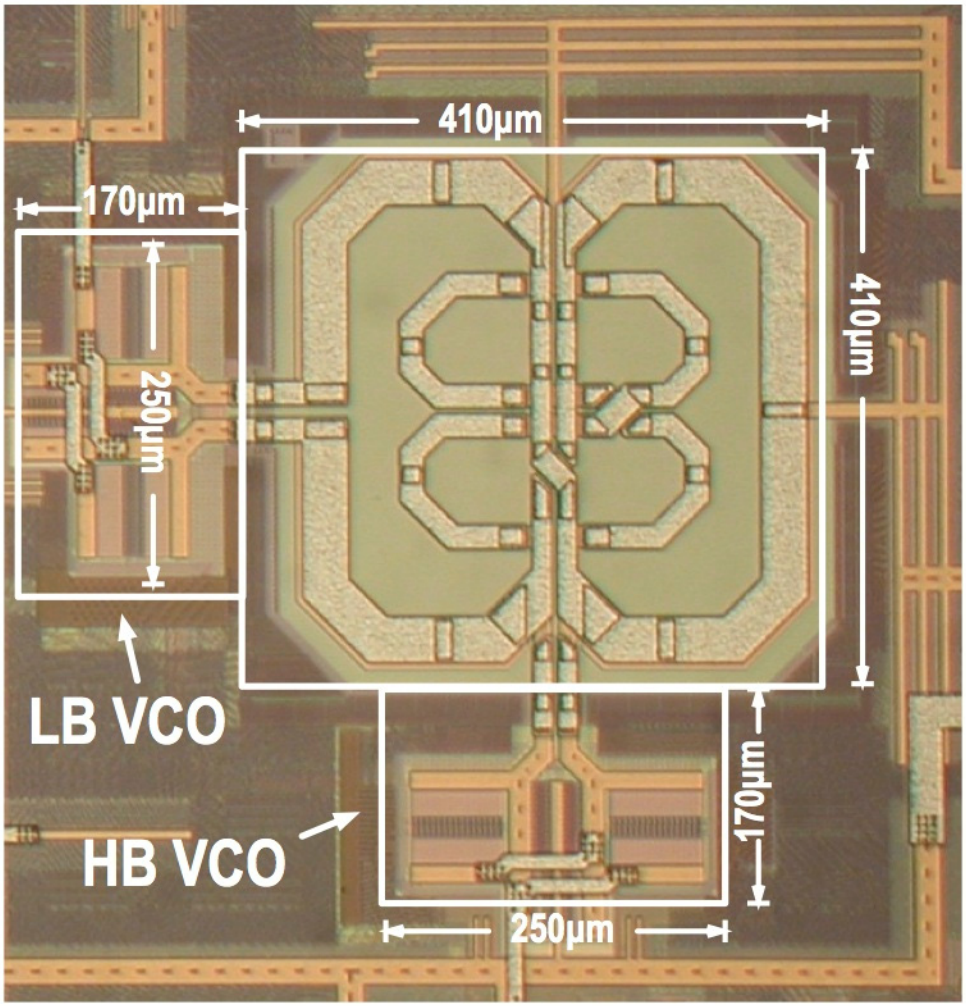
Dual-Core class-D VCO



- Orthogonal 8-shaped inductor → no magnetic field between coils
- Very wide tuning range with small inductor area
- Class-D VCOs → low voltage supply, high performance

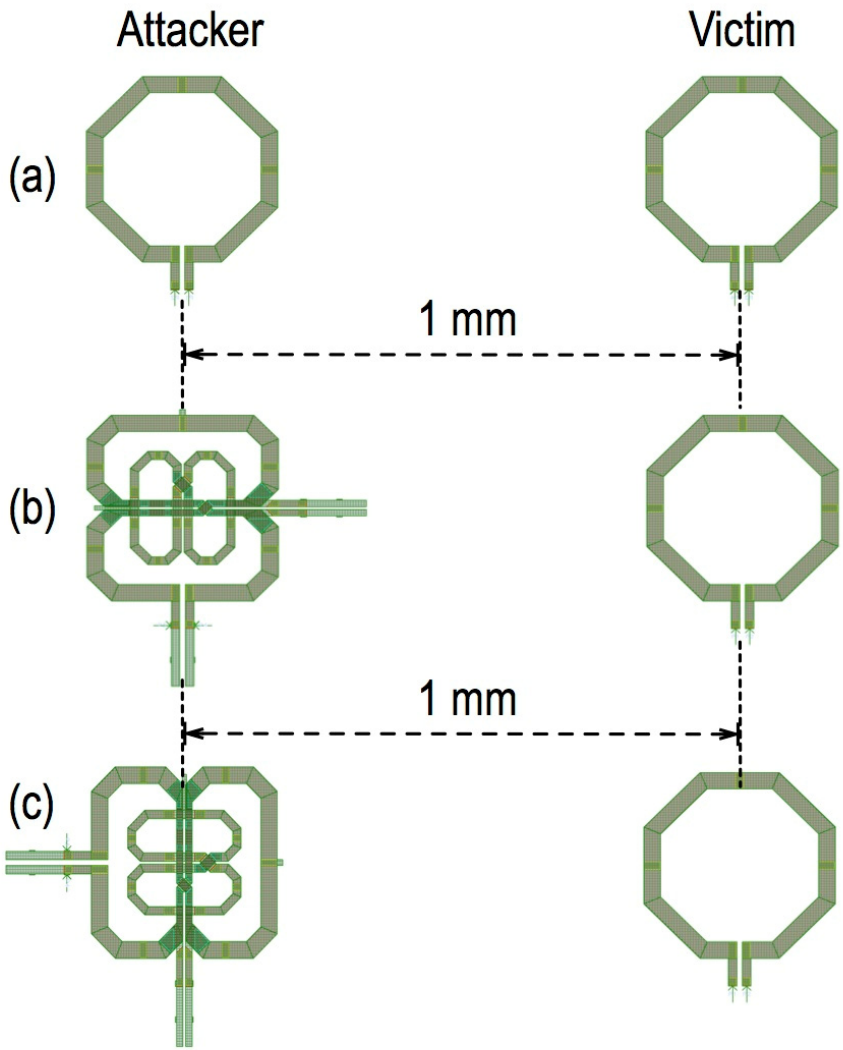
Fanori and Andreani, JSSC'13

Die photograph



- 65nm CMOS process without thick metal
- Inductors: 1nH and 0.6nH
- Overall tuning range: 2.4-5.3GHz (75%)
- 0.33mm^2 active area
- Voltage supply: 0.4-0.5V

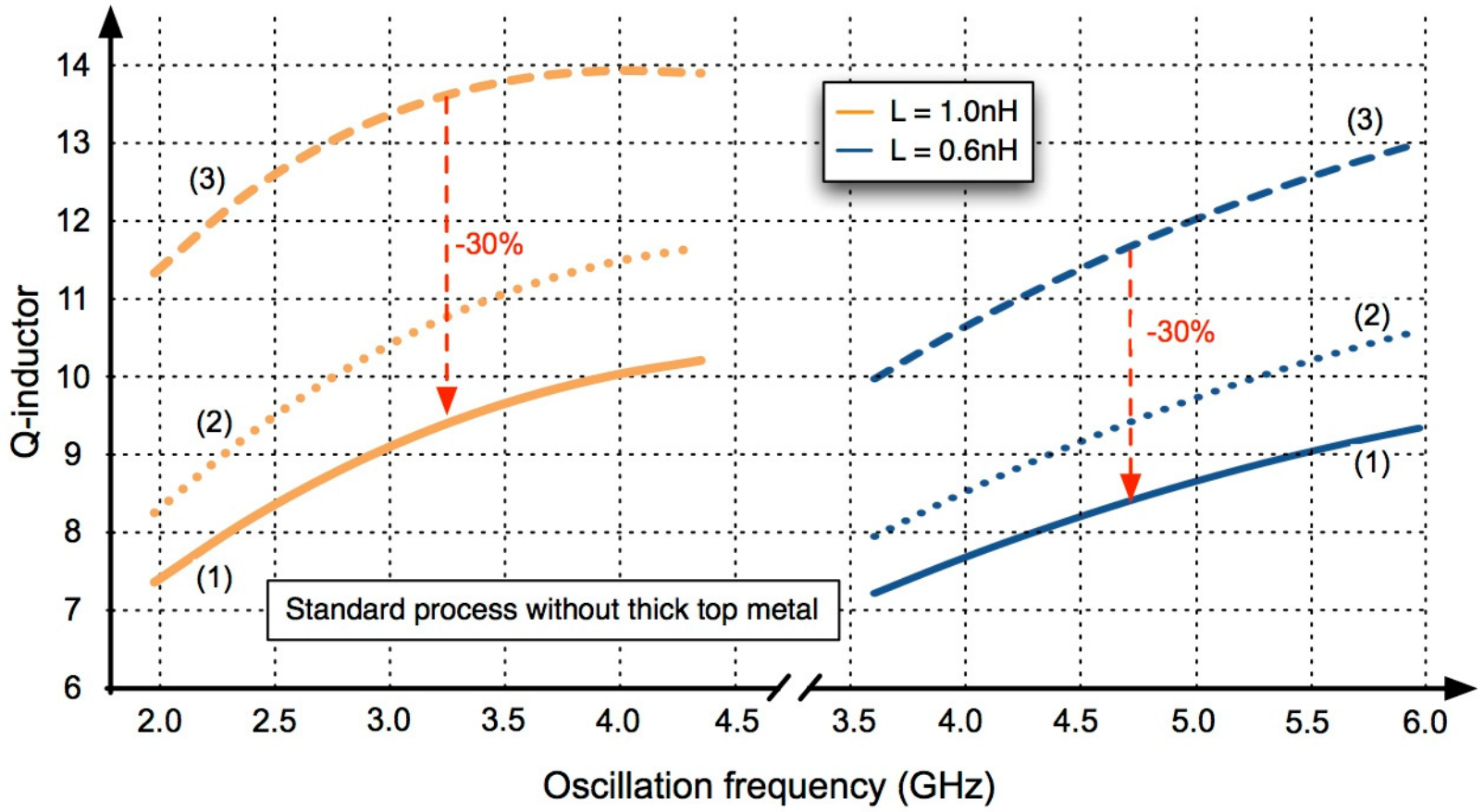
Concentric 8-shaped vs. octagonal inductors



	S_{21} at Victim
(a)	reference
(b) Large coil	**-31dB**
(b) Small coil	**-15dB**
(c) Large coil	**-17dB**
(c) Small coil	**-45dB**

Concentric 8-shaped coils do not compromise pulling rejection

Q vs. frequency

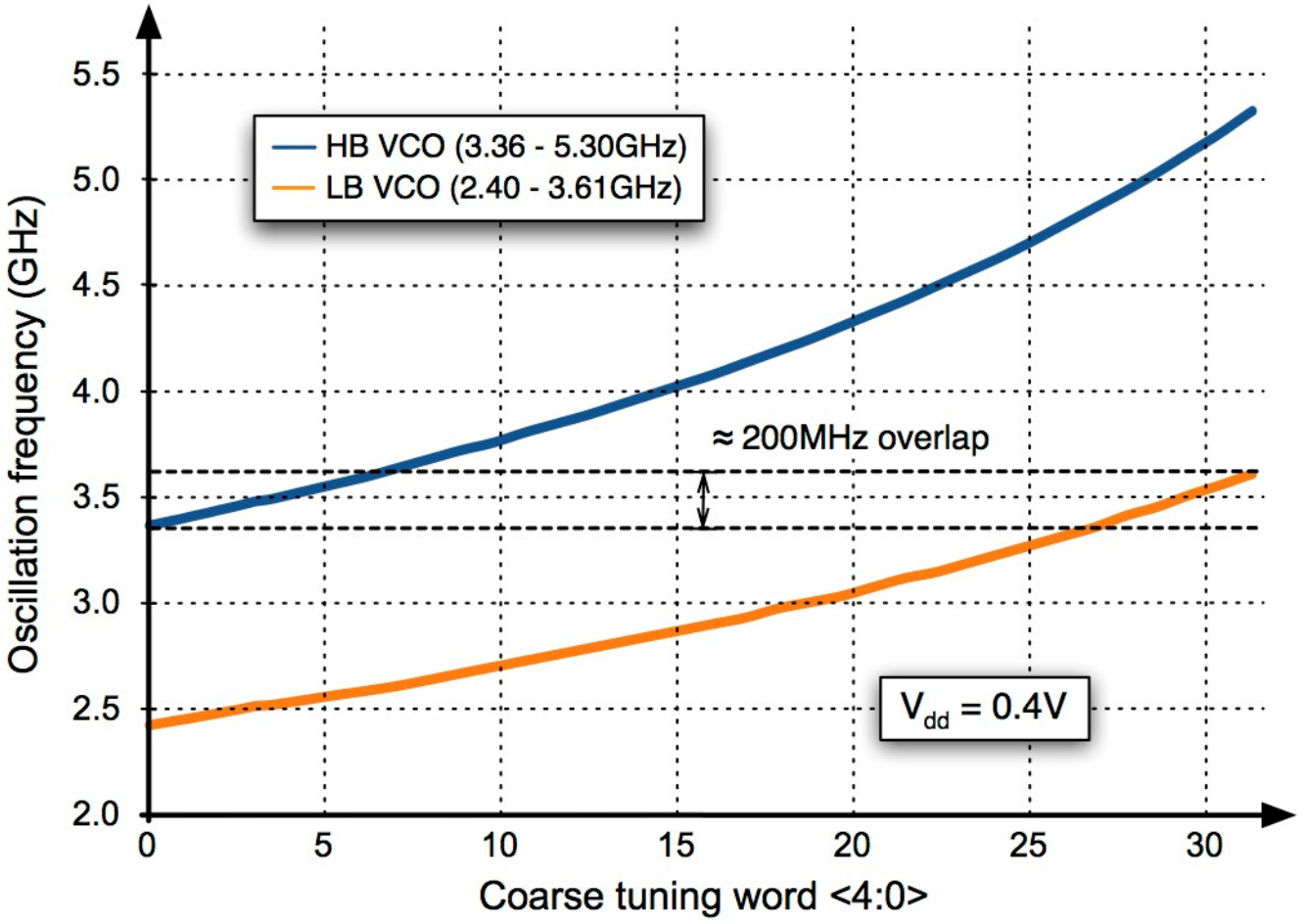


(1) Actual design

(2) Other inductor removed (difference < 10%)

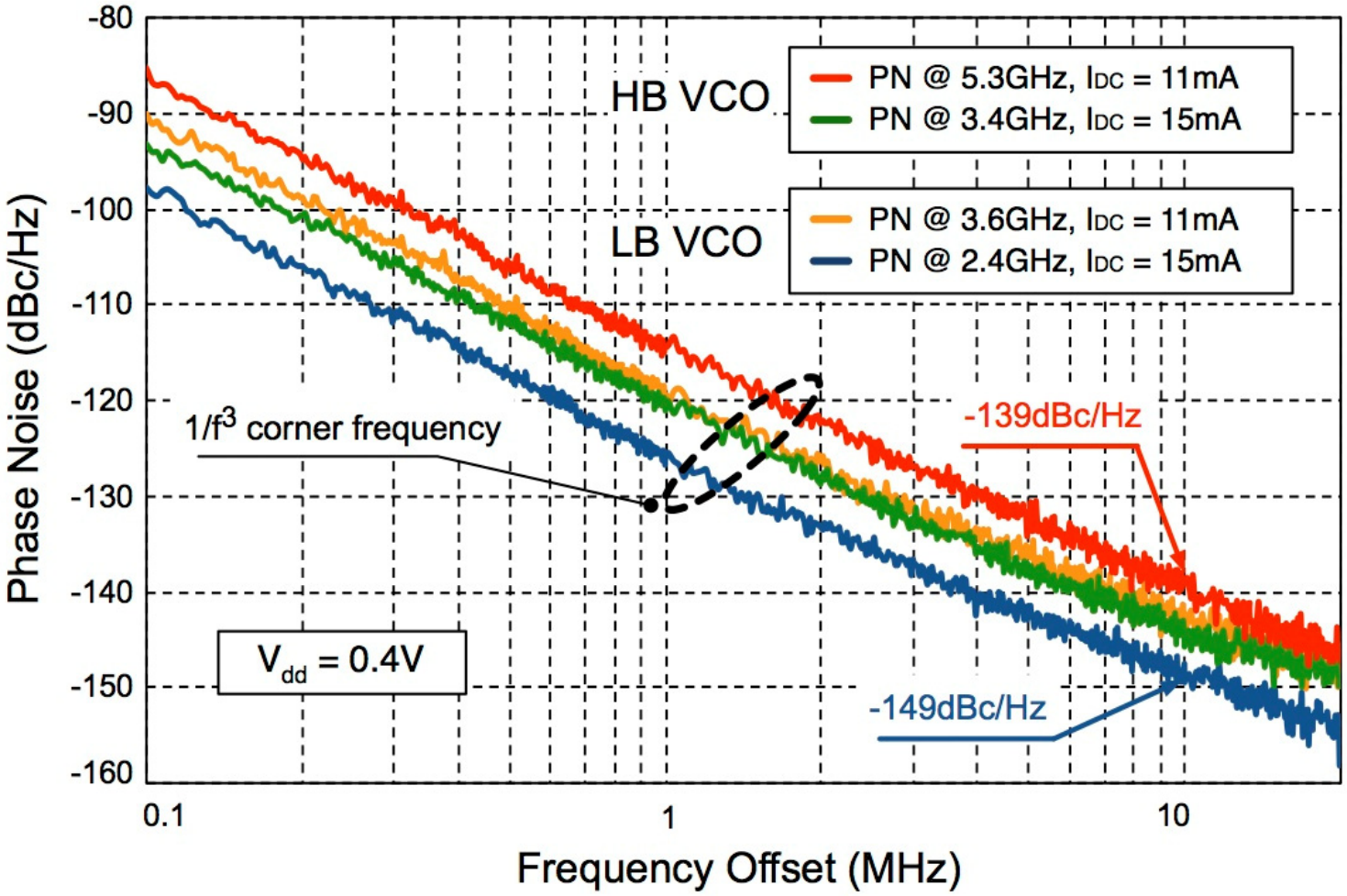
(3) Inductor optimized for standalone VCO

Tuning range



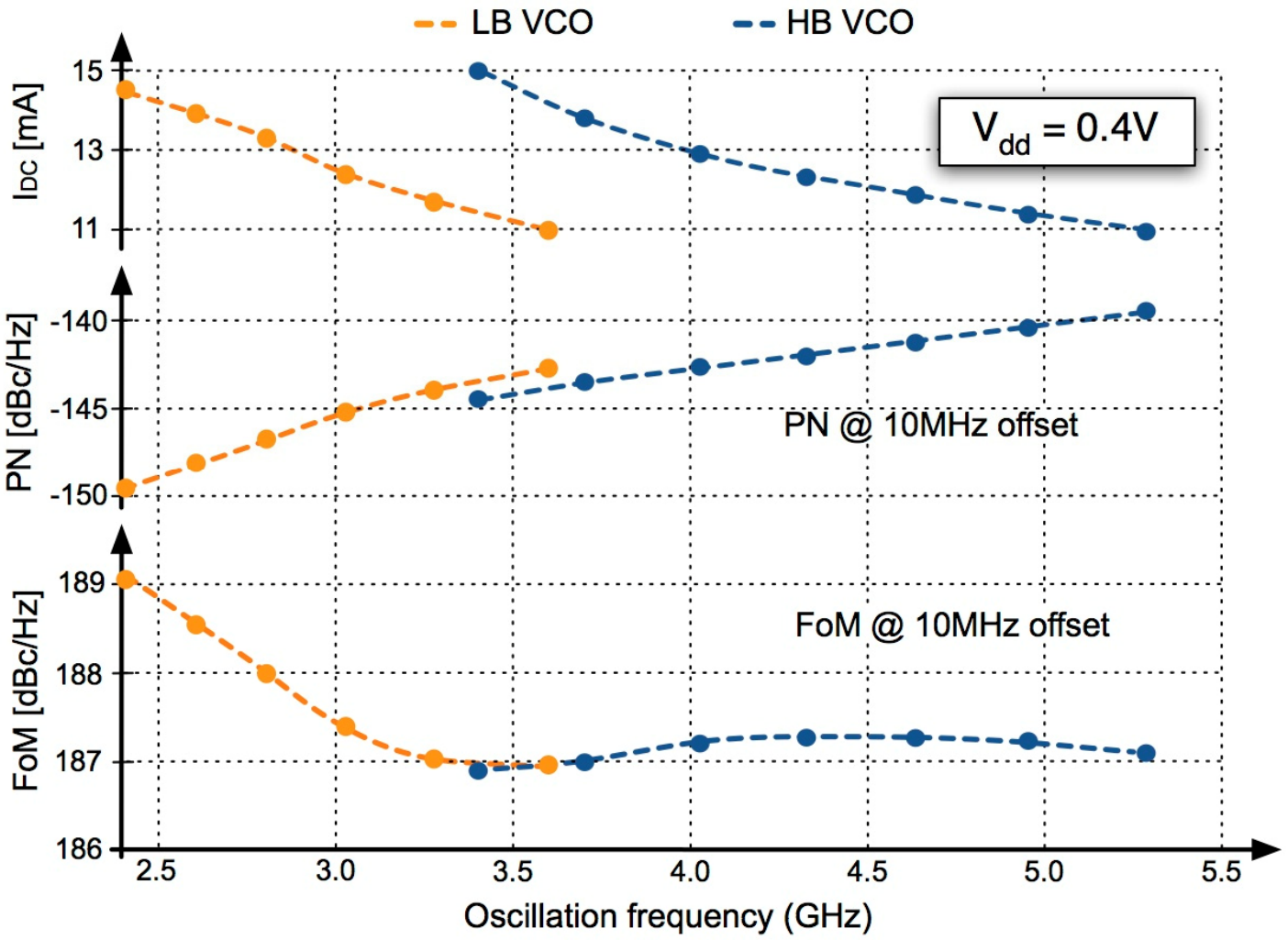
75% tuning-range with 200MHz overlap

Phase noise measurements



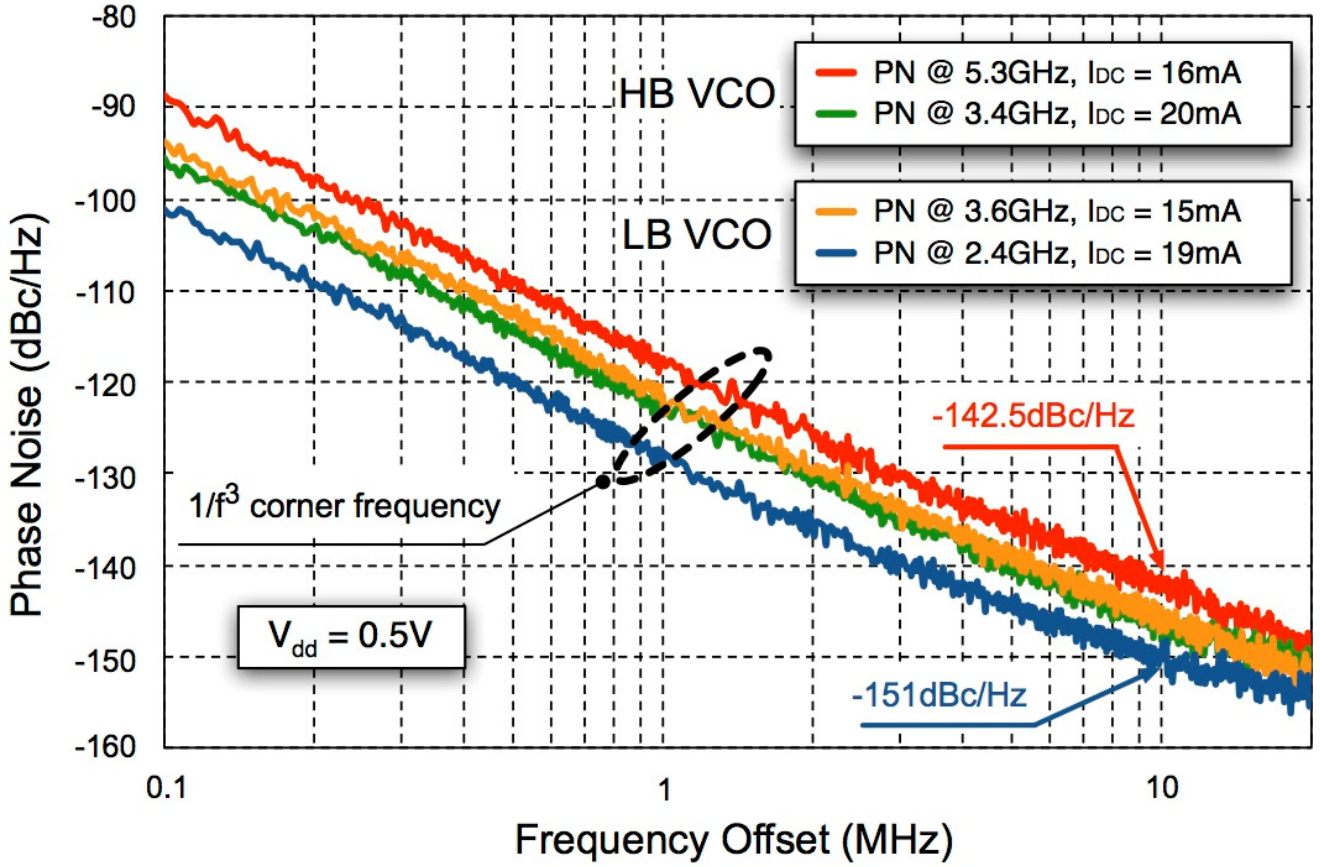
- FoM ≈ 187/189dBc/Hz across the tuning range
- 1/f^3 noise corner frequency between 1MHz and 2MHz

Performance vs. f_{osc}



The FoM varies 2dB across tuning range

Phase noise measurements V_{dd}= 0.5V



- Higher V_{dd} improves switches performance and phase noise
- FoM ≈ 188/189dBc/Hz across the tuning range
- 1/f^3 noise corner frequency between 0.7MHz and 1.5MHz

State of the art

	Frequency (GHz)	Overlap (MHz)	Supply (V)	Phase Noise (dBc/Hz)	P_{DC} (mW)	FoM (dBc/Hz)
This work	**2.4 – 3.6 3.4 – 5.3 (75%)**	**200**	**0.4**	**-149 @2.4GHz -139 @5.3GHz offset 10MHz**	**6.0 – 4.4**	**187–189**
Li, *JSSC '12*	2.5 – 3.9 3.3 – 5.6 (76%)	600	0.6	-157 @3.7GHz -152 @5.5GHz offset 20MHz	9.5 – 14	188–192
Sadhu, *CICC '09*	3.3 – 6.0 5.6 – 8.3 (86%)	400	1.6	-122 @3.3GHz -117 @8.3GHz offset 1MHz	15.5 – 6.5	181–187
Ruippo, *MWCL '10*	2.9 – 4.8 4.7 – 5.4 (60%)	100	1.8	-128 @2.9GHz -122 @5.4GHz offset 1MHz	13.5 – 9.8	185–190
Andreani, *JSSC '11*	2.5 – 4.0 4.9 – 5.8 (47% – 17%)	–	1.2	-156 @3.8GHz -146 @5.8GHz offset 20Mhz	23 – 25.5	188 – 182
Borremans, *JSSC '08*	3.1 – 4.0 8.8 – 11.2 (25% – 24%)	–	1.2	-122 @3.9GHz -117 @10.9GHz offset 2.5MHz	10 – 2.2	181 – 182

Conclusions

- LTE with RX/TX carrier aggregation requires 4 PLLs with large tuning range working simultaneously
- High CMOS costs impose area reduction, aggravating pulling
- Dual-core VCO with concentric 8-shaped inductors yields 75% tuning range saving 30% area
- FoM = 187-189dBc/Hz across the tuning range

Acknowledgements

We are very grateful to STMicroelectronics for silicon donation.

This work has been partially funded by SSF under the DARE project, and by the European Marie Curie Project FP7-PEOPLE-2009-IAPP n° 251399

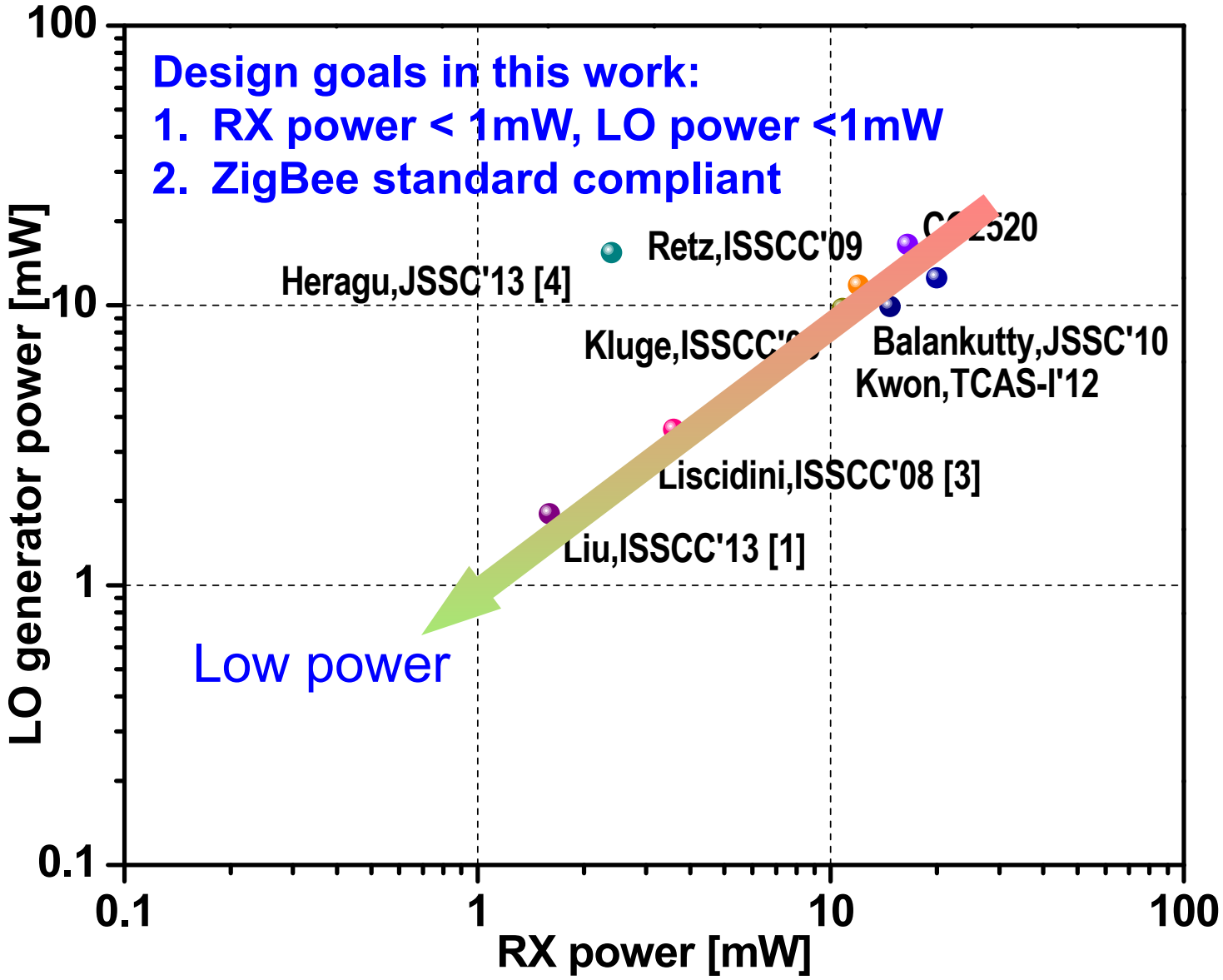
A 1.8mW PLL-Free Channelized 2.4GHz ZigBee Receiver Utilizing Fixed-LO Temperature-Compensated FBAR Resonator

Keping Wang, Jabeom Koo, Richard Ruby*, Brian Otis
University of Washington, Seattle, WA
*Avago Technologies, San Jose, CA

Outline

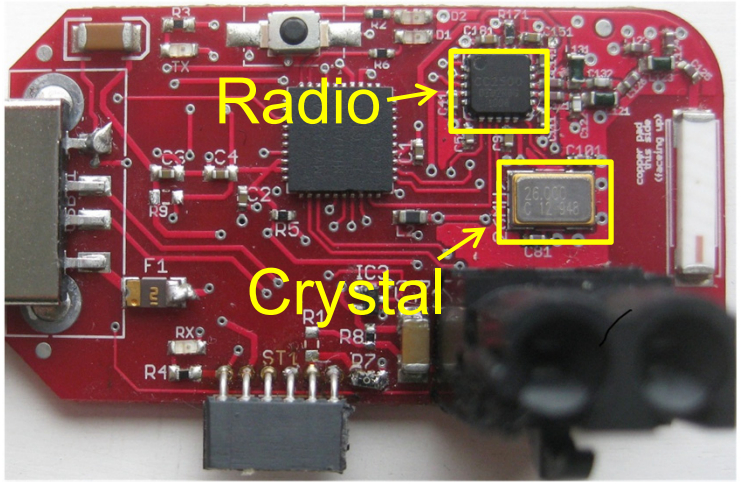
- Motivation
- ZigBee Receiver Prior Art
- Proposed Receiver Architecture
- Circuit Implementation
- Experimental Results
- Conclusion

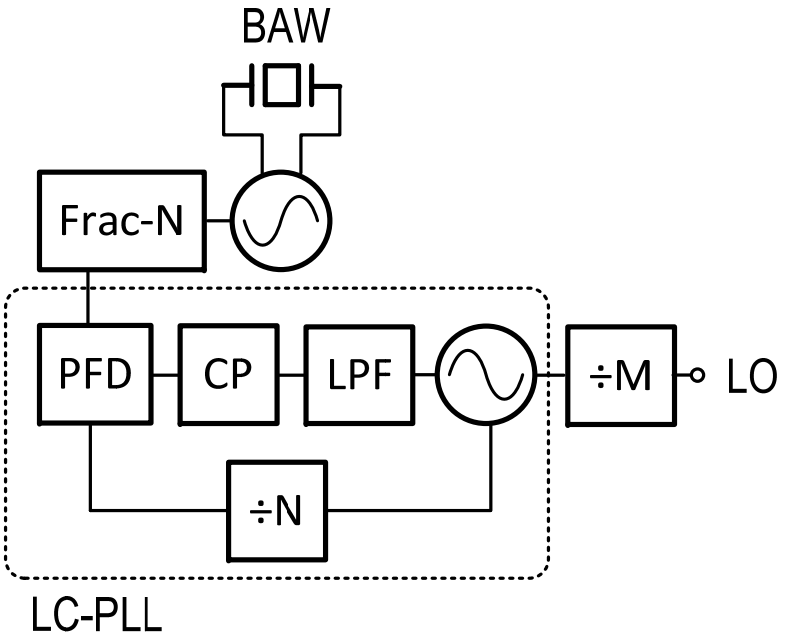
Benchmark with Prior Art



2.4GHz LO Generator Prior Art

- PLL-based radio
  - Bulky crystal
  - Power-hungry
- MEMS-based radio
  - Power-hungry
  - Area-hungry

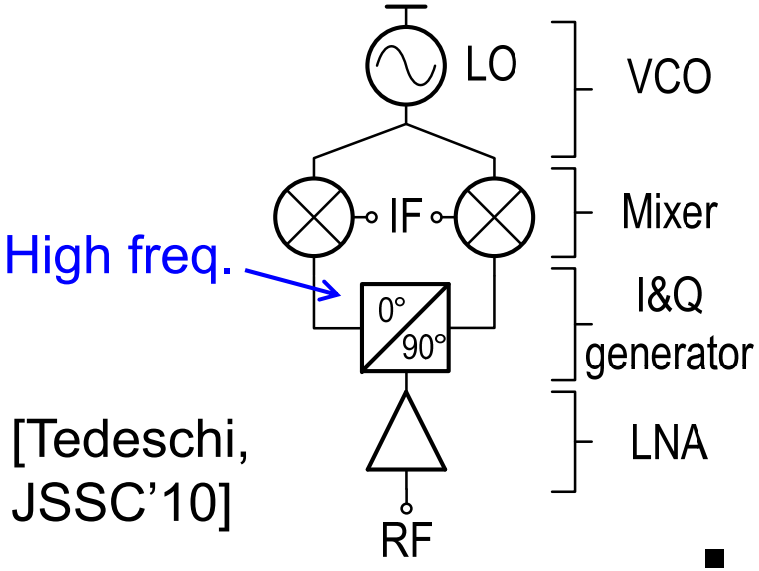




[Heragu, JSSC'13]

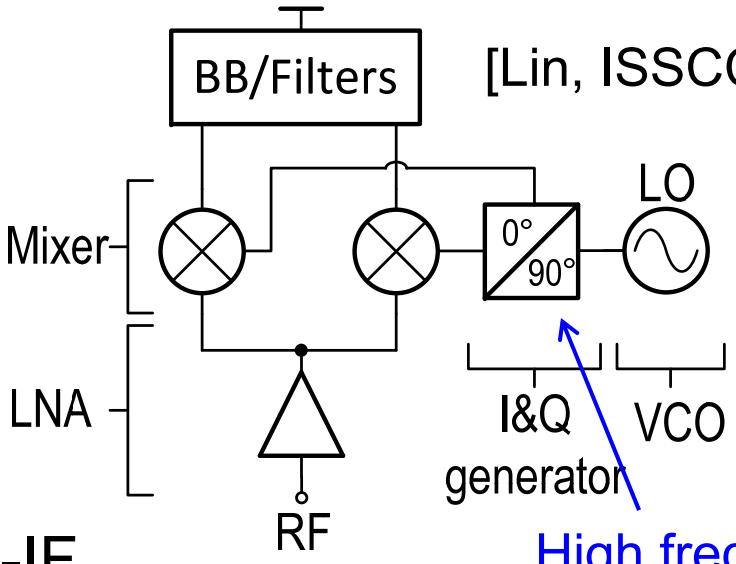
Receiver Architecture Prior Art

- Low-IF with LMV

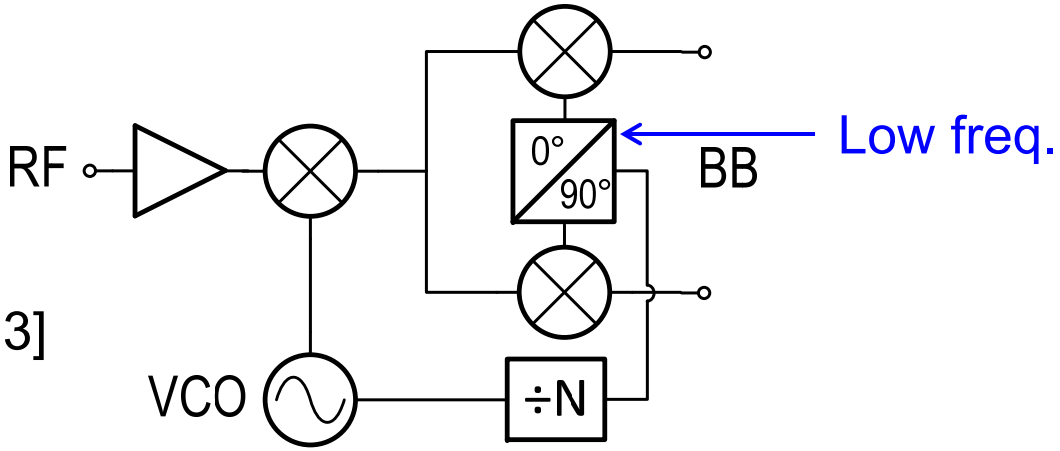


[Tedeschi, JSSC'10]

- Low-IF with Blixer



- Sliding-IF

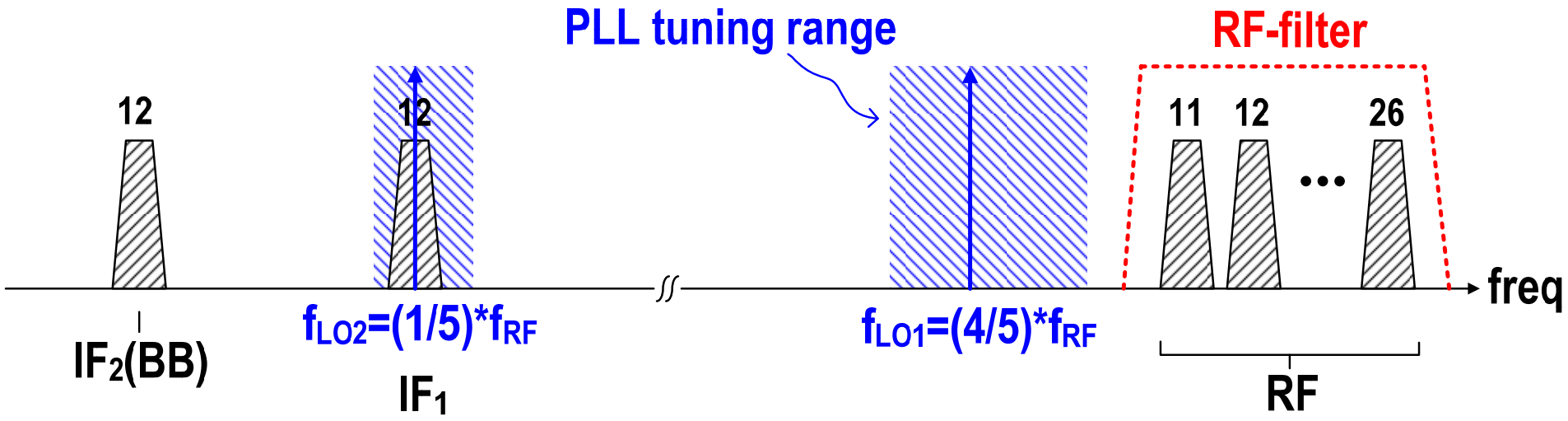


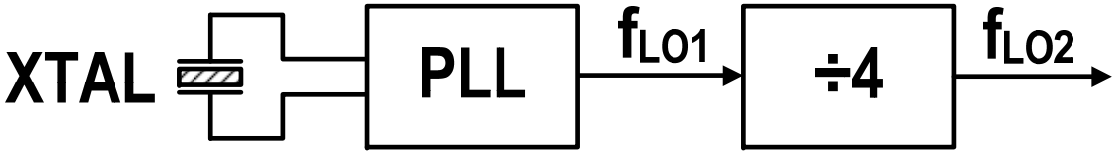
[Liu, ISSCC'13]

Proposed Receiver Techniques

- **Sliding-IF receiver architecture**
  - Avoid high freq. quadrature LO
- **Utilize FBAR-based quartz-free LO generator**
  - FBAR: thin-film bulk acoustic-wave resonator
  - 30dB power/PN benefit
  - Introduce fixed-LO freq. plan
  - Channelized by integer-N multi-mode dividers (MMD)
- **Current-reuse technique**
  - LNA, Mixer, Filter, PGAs

Frequency Plan (1)





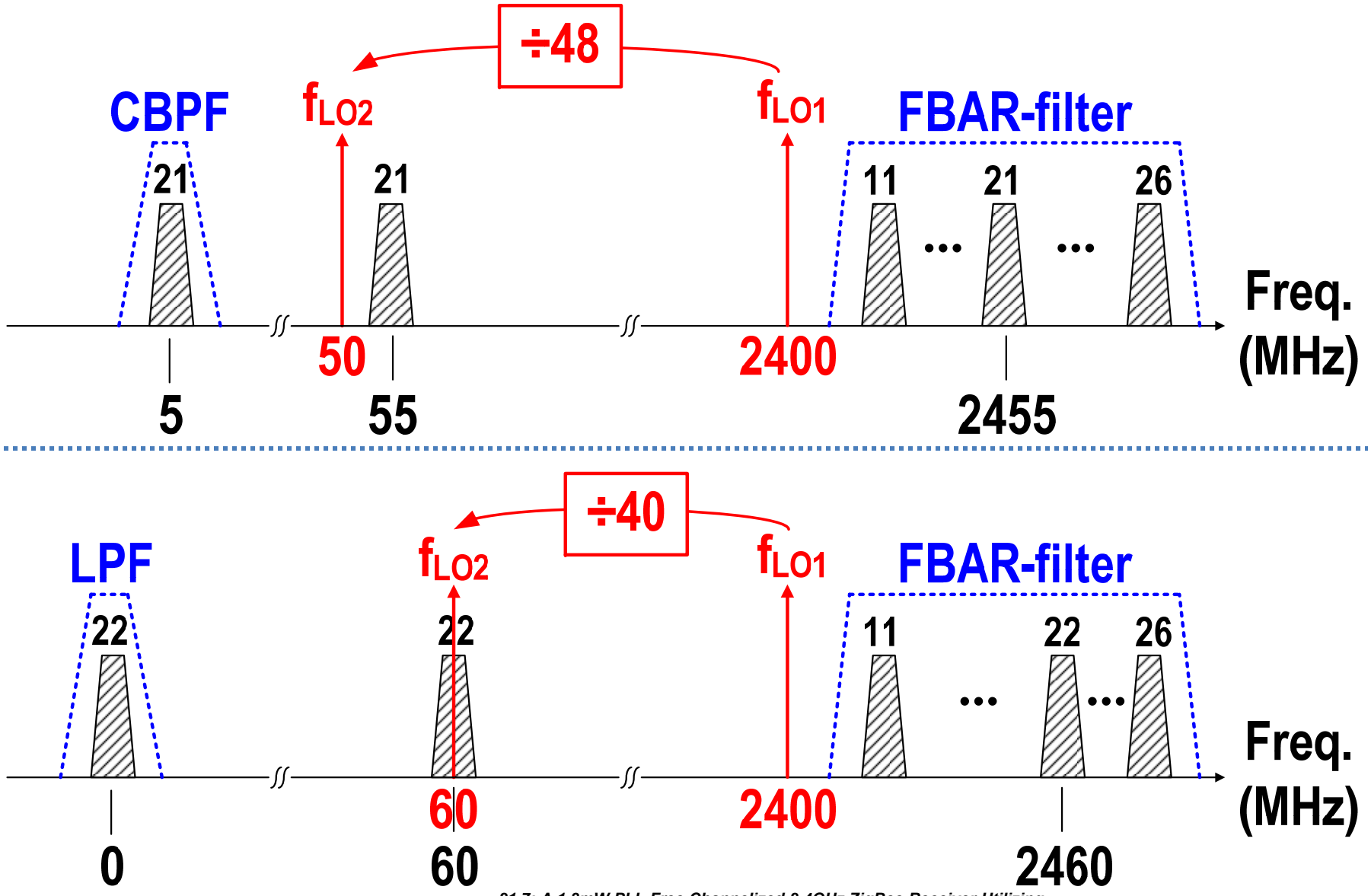
Traditional Sliding-IF

Proposed Sliding-IF

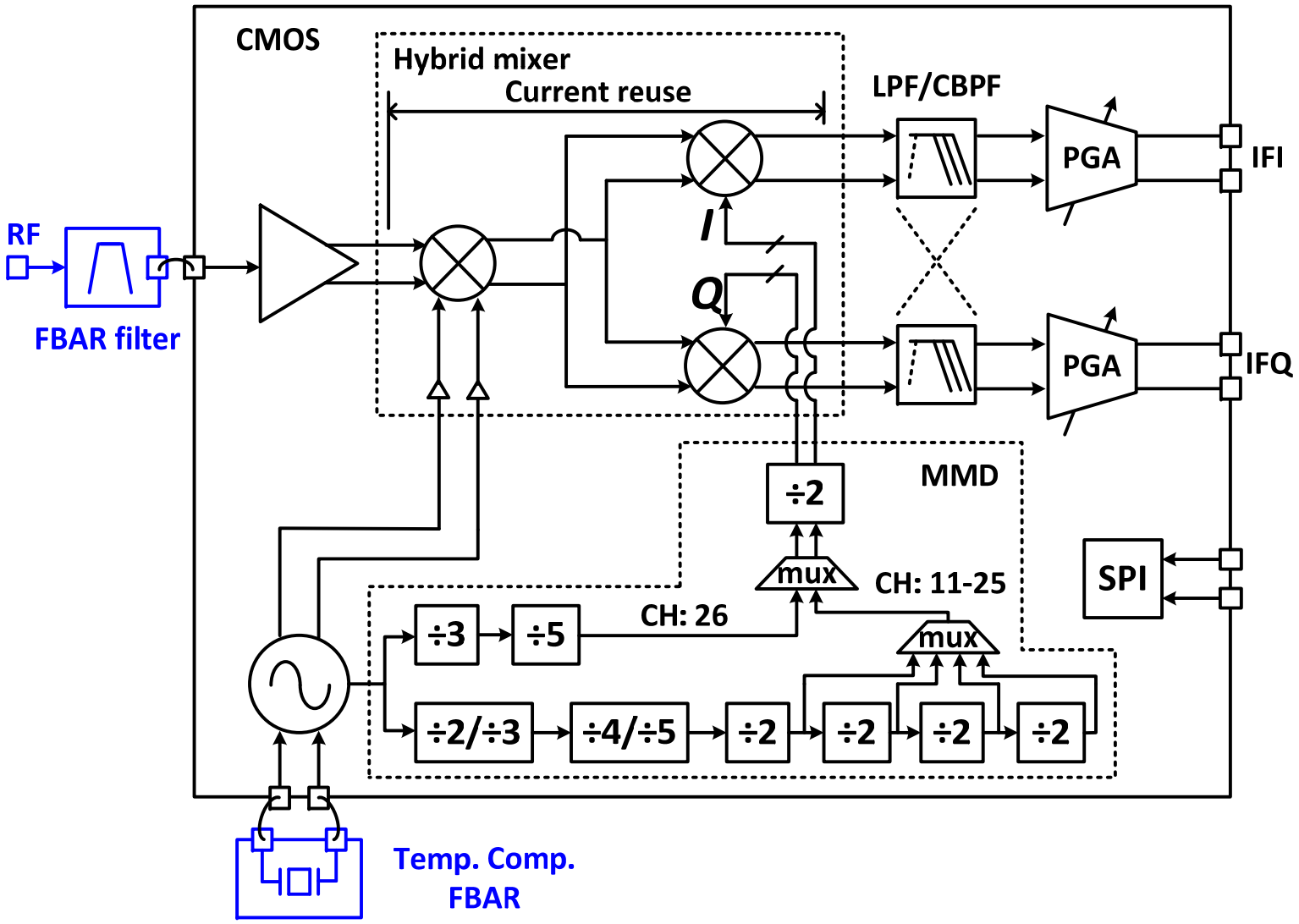
Frequency Plan (2)

Channel #	RF (MHz)	1st LO (MHz)	1st IF (MHz)	2nd LO (MHz)	2nd IF (MHz)	MMD division radio (1st LO/2nd LO)
11	2405	2400	5	5	0	480
12	2410		10	10	0	240
13	2415		15	15	0	160
14	2420		20	20	0	120
15	2425		25	25	0	96
16	2430		30	30	0	80
17	2435		35	30	5	80
18	2440		40	40	0	60
19	2445		45	40	5	60
20	2450		50	50	0	48
21	2455		55	50	5	48
22	2460		60	60	0	40
23	2465		65	60	5	40
24	2470		70	75	5	32
25	2475		75	75	0	32
26	2480		80	80	0	30

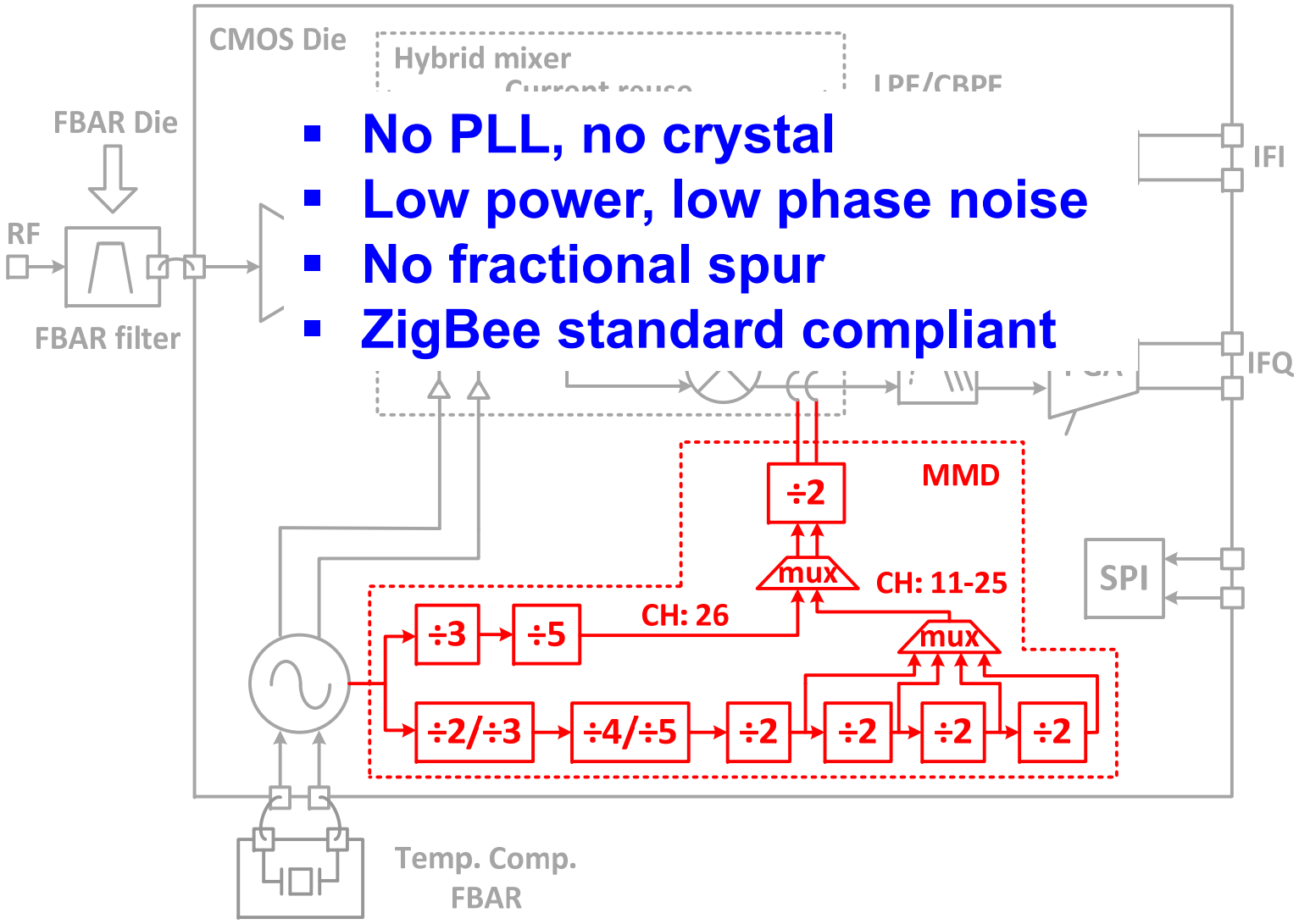
Frequency Plan (3)



ZigBee Receiver Architecture

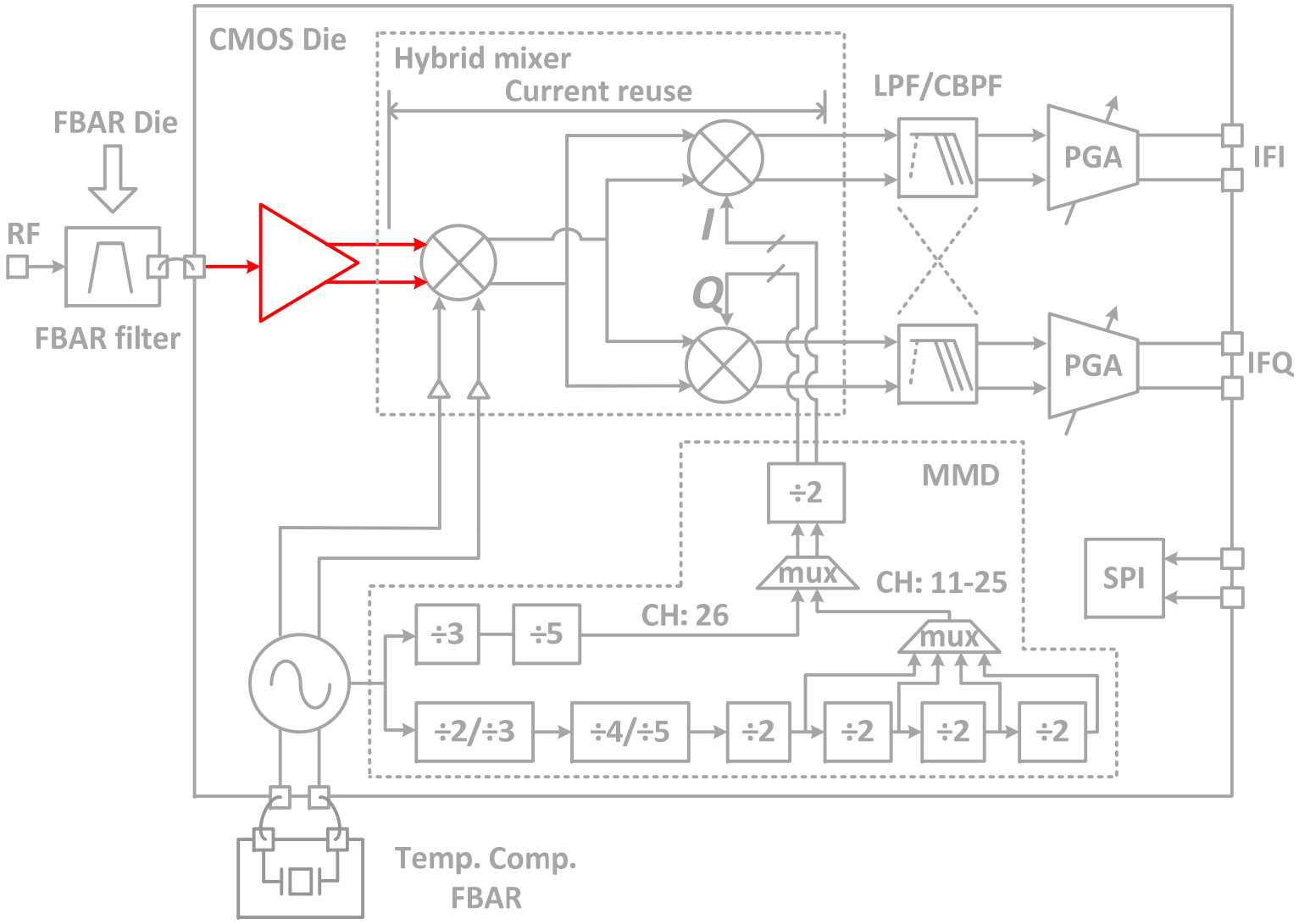


Multi-mode Divider



- No PLL, no crystal
- Low power, low phase noise
- No fractional spur
- ZigBee standard compliant

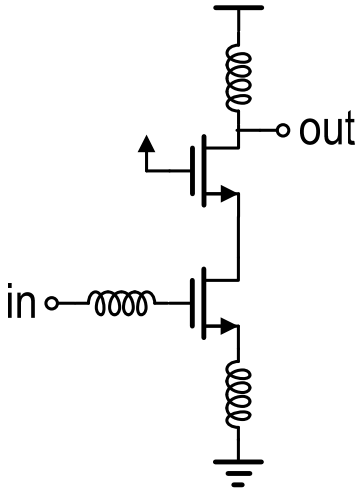
Low Power LNA Design



LNA Prior Art (1)

- **Inductive source degeneration LNA**

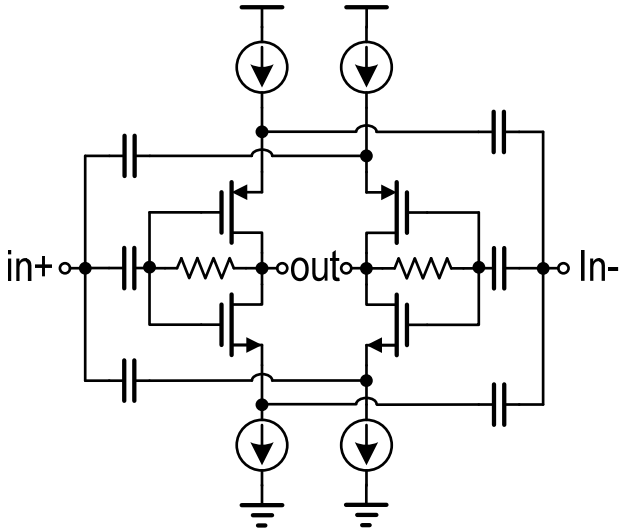
✓ Very low NF
✗ Moderate power
✗ Narrow-band matching
✗ Need inductors



[Shaeffer, JSSC'97]

- **CG shunt-feedback LNA**

✓ No inductor needed
✗ Differential RF input

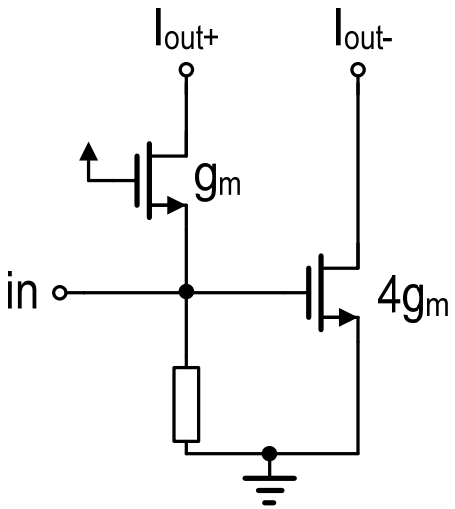


[Wang, JSSC'06]

LNA Prior Art (2)

- **CG-CS balun LNA**

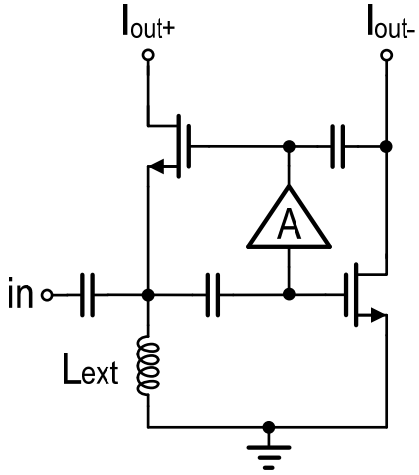
✓ Wide-band matching
✓ Low NF
✗ Output Imbalance
✗ High power



[Blaakmeer, JSSC'08]

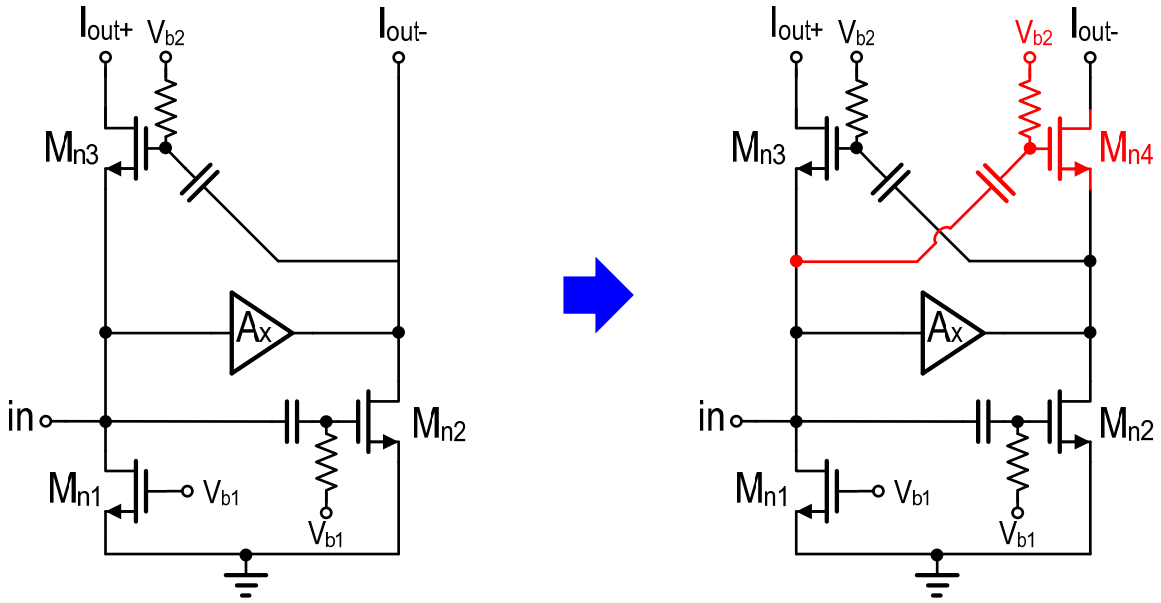
- **CG-CS g_m-boost balun LNA**

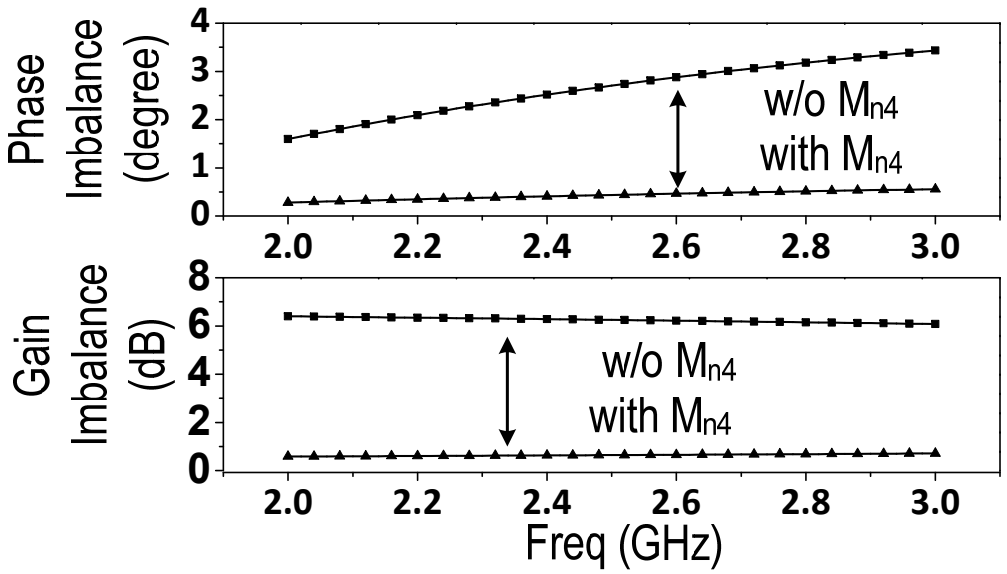
✓ Wide-band matching
✓ Low NF
✗ Need external inductor
✗ Moderate power



[Mak, JSSC'11]

Proposed Current-reuse LNA (1)

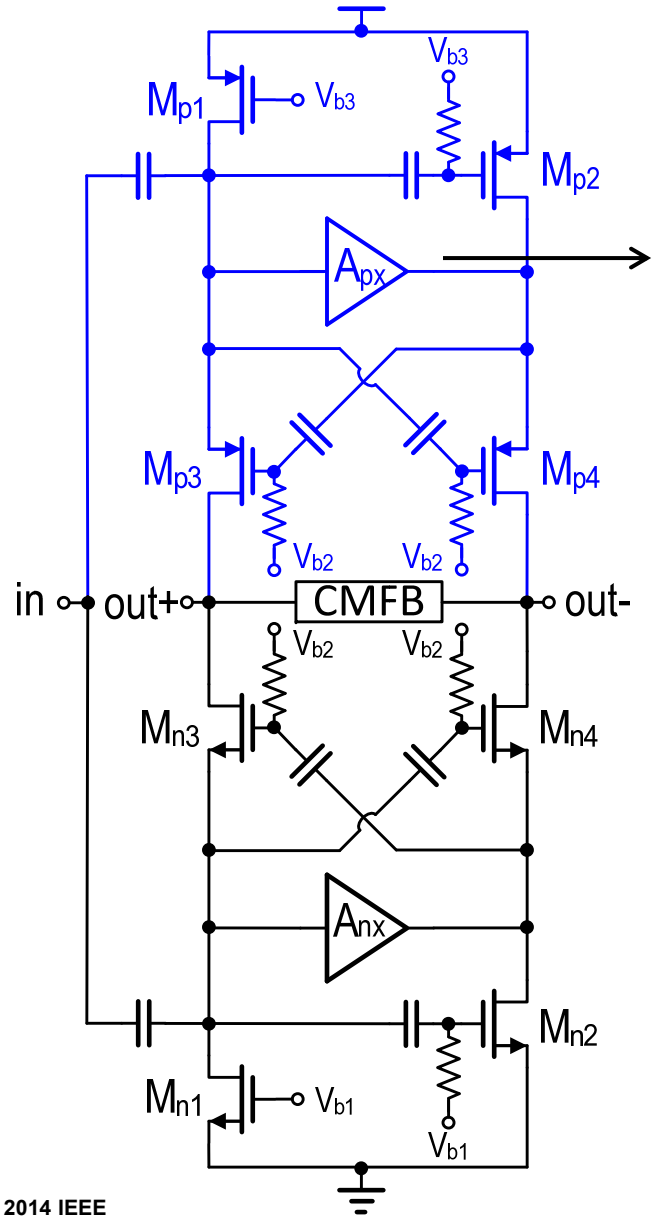


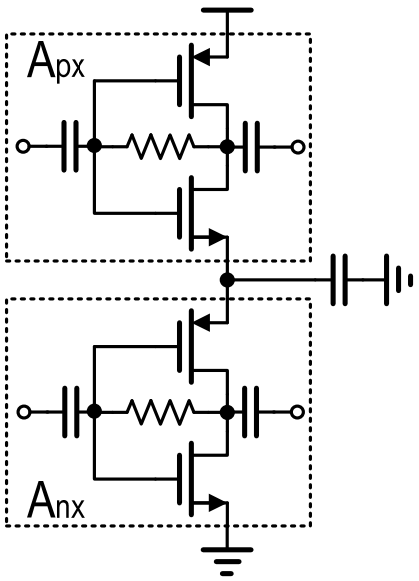


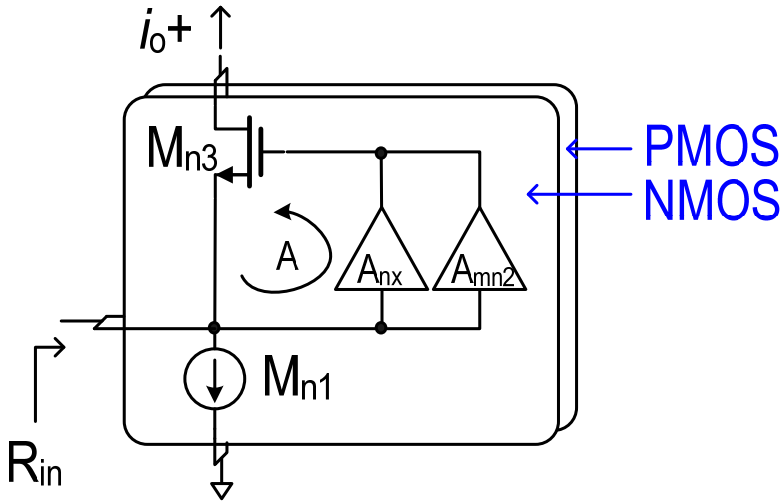
Phase-imbalance
2.2° improved

Gain-imbalance
5.6dB improved

Proposed Current-reuse LNA (2)





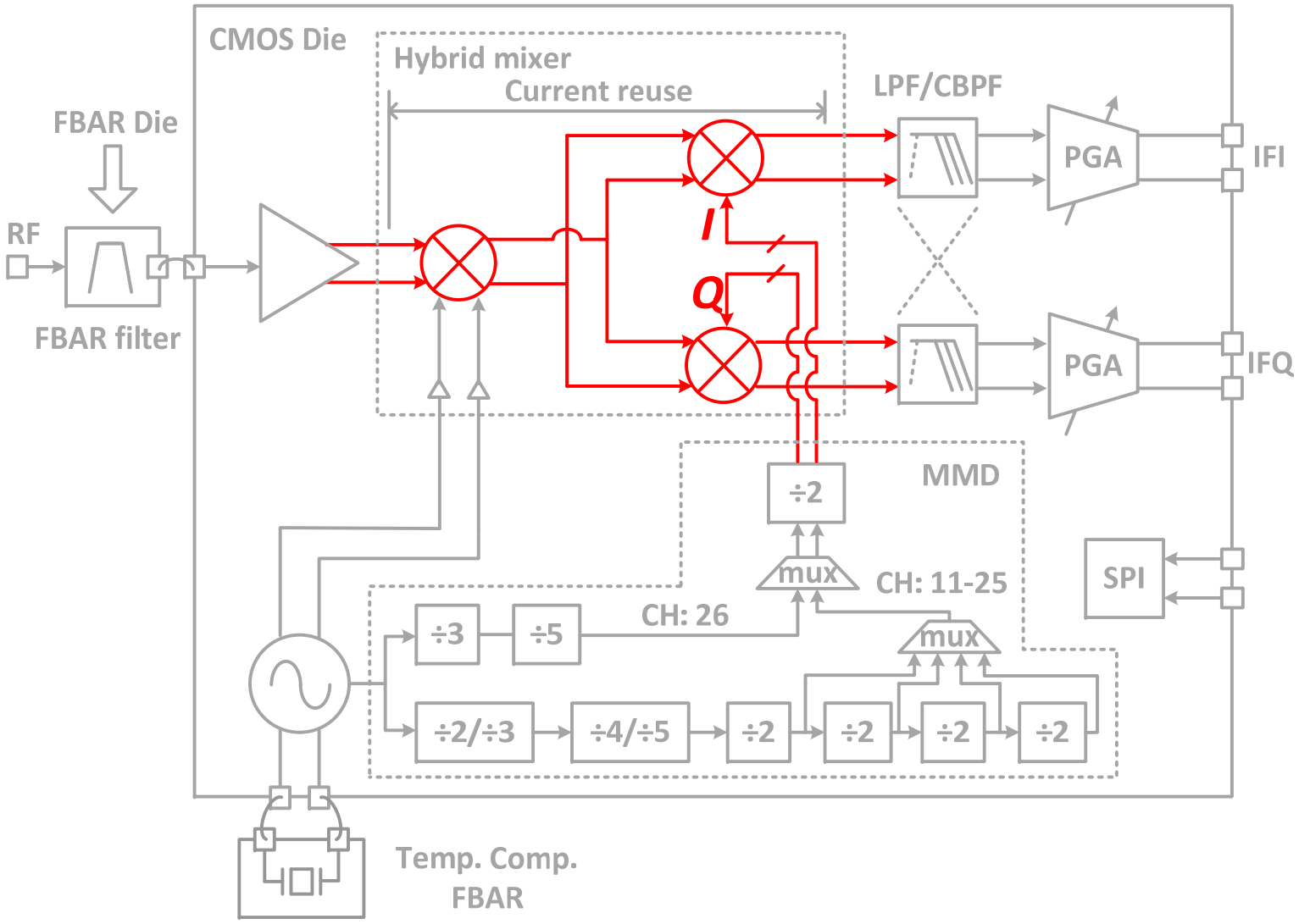


$$A = A_{nx} + A_{mn2}$$

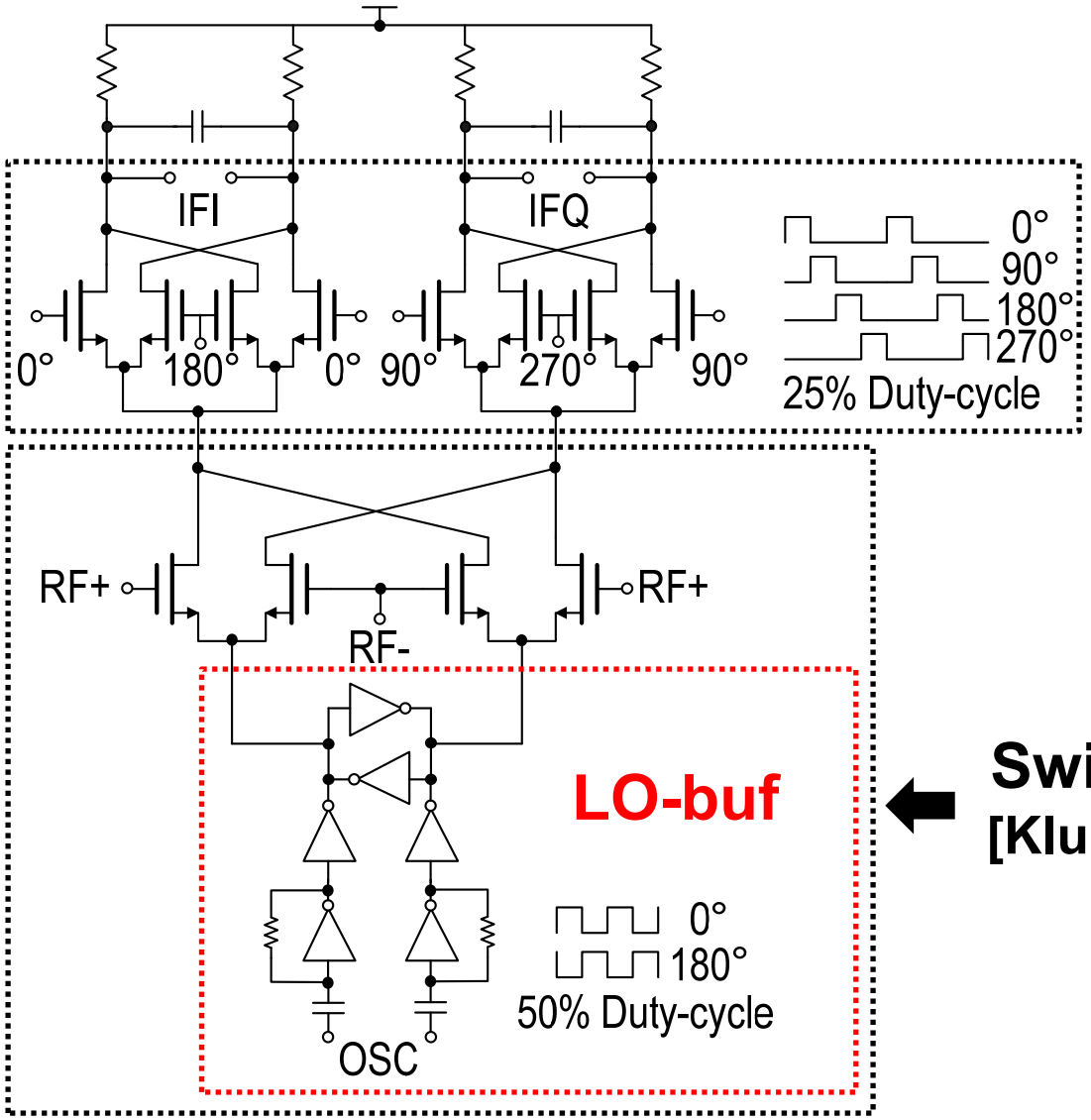
$$R_{in} \approx 1/(2 * g_{mn3} * (1+A))$$

- 2*(1+A) times lower current than traditional CG-CS.

Proposed Hybrid Mixer



Proposed Hybrid Mixer

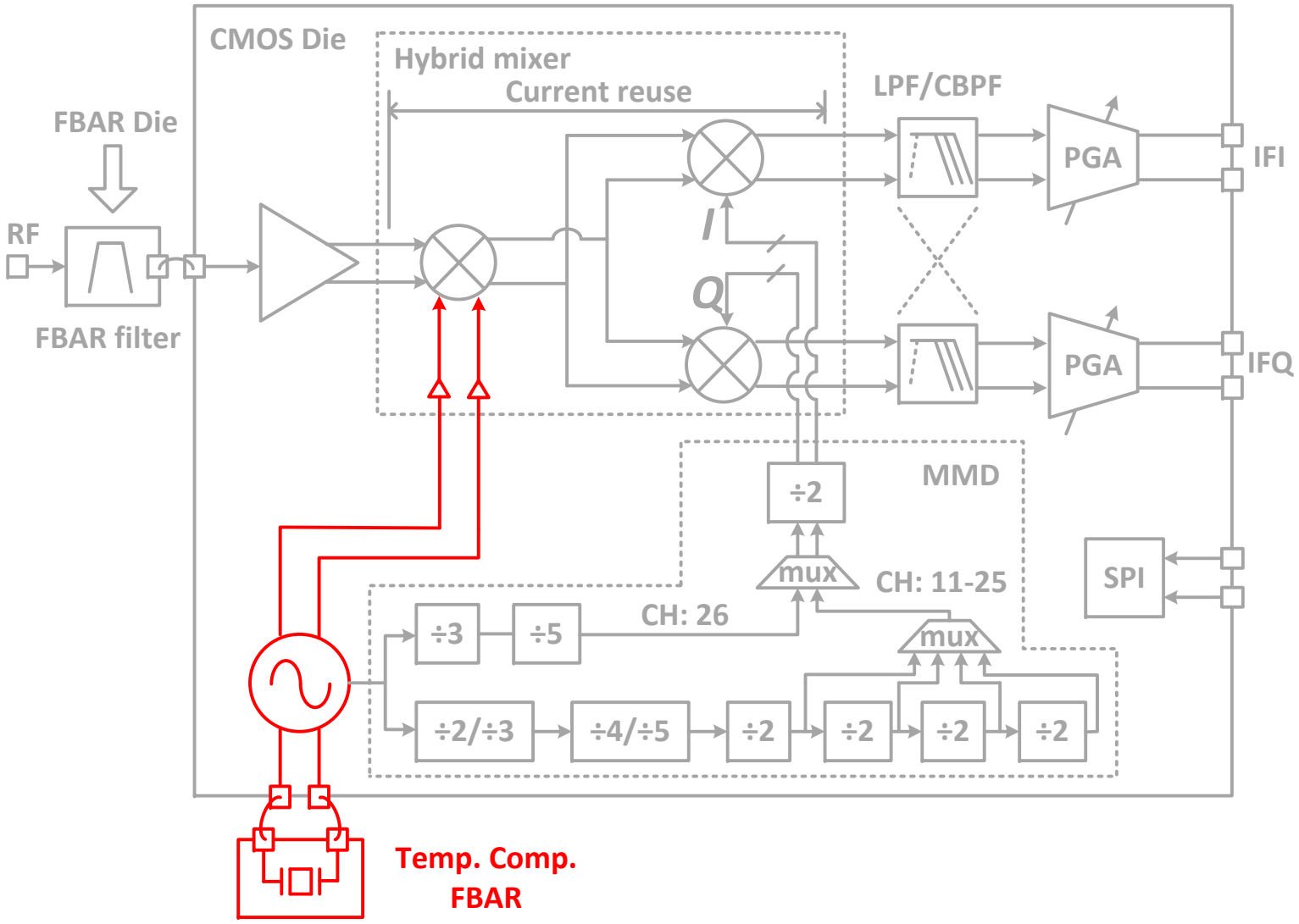


Switch stage

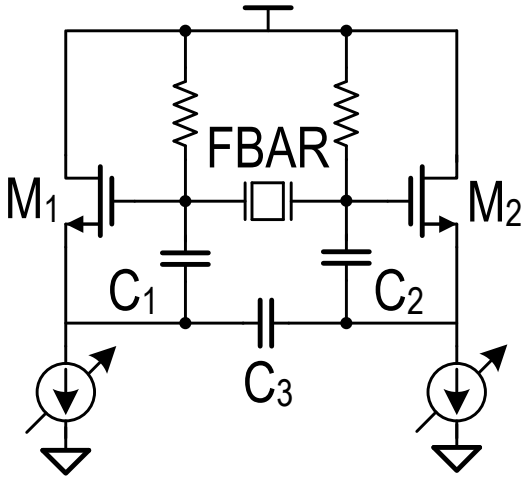
Current-reuse

Switched-g_m stage
[Klumperink, JSSC'04]

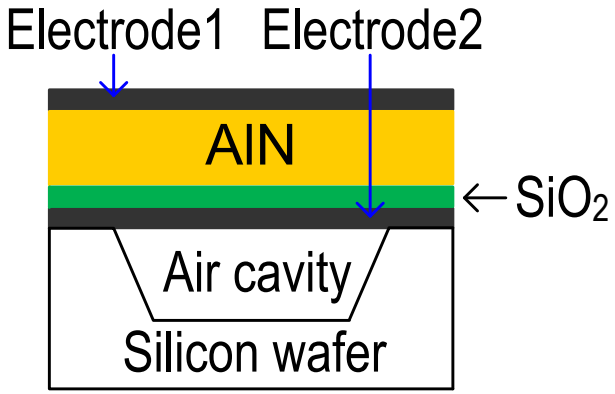
FBAR Oscillator



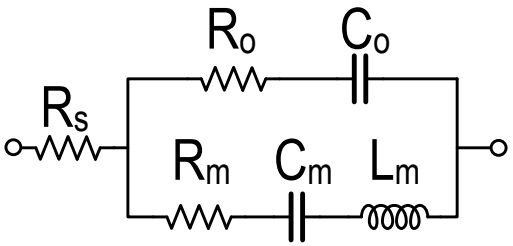
FBAR Oscillator



<Differential Colpitts>



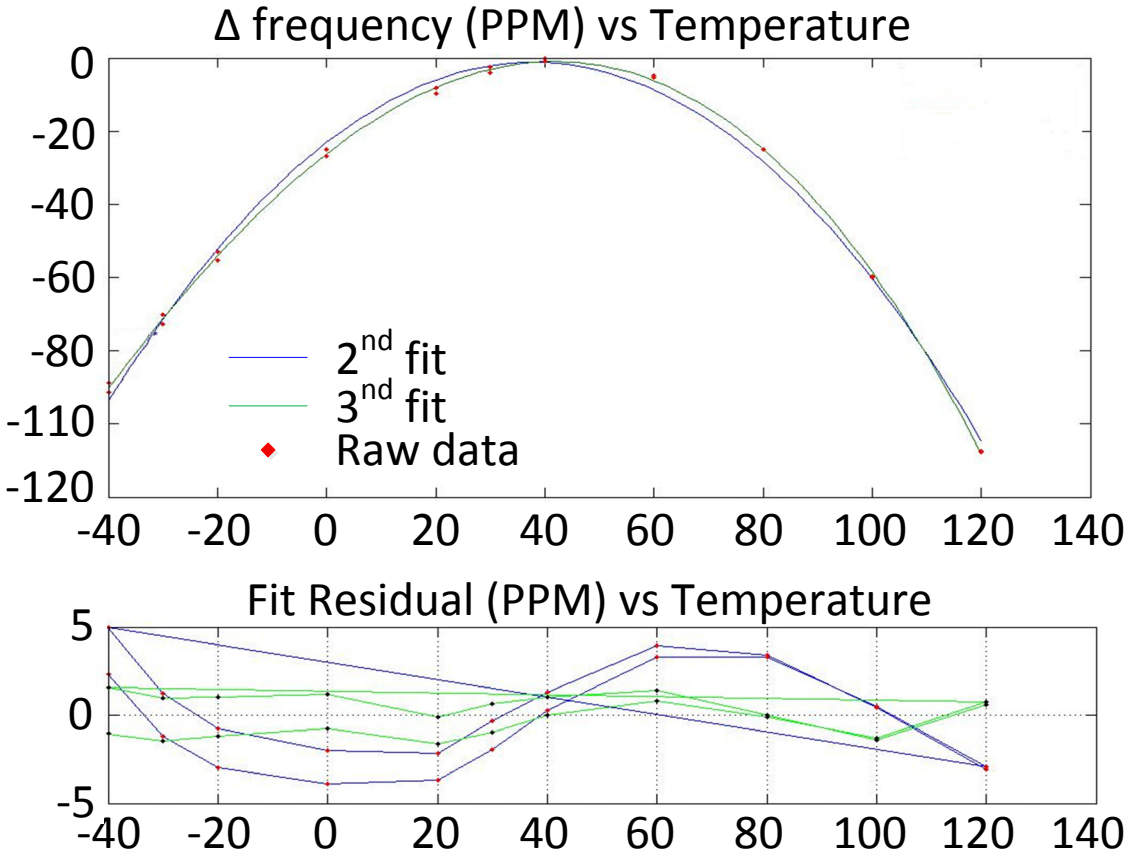
<FBAR cross-section>



<mBVD model>

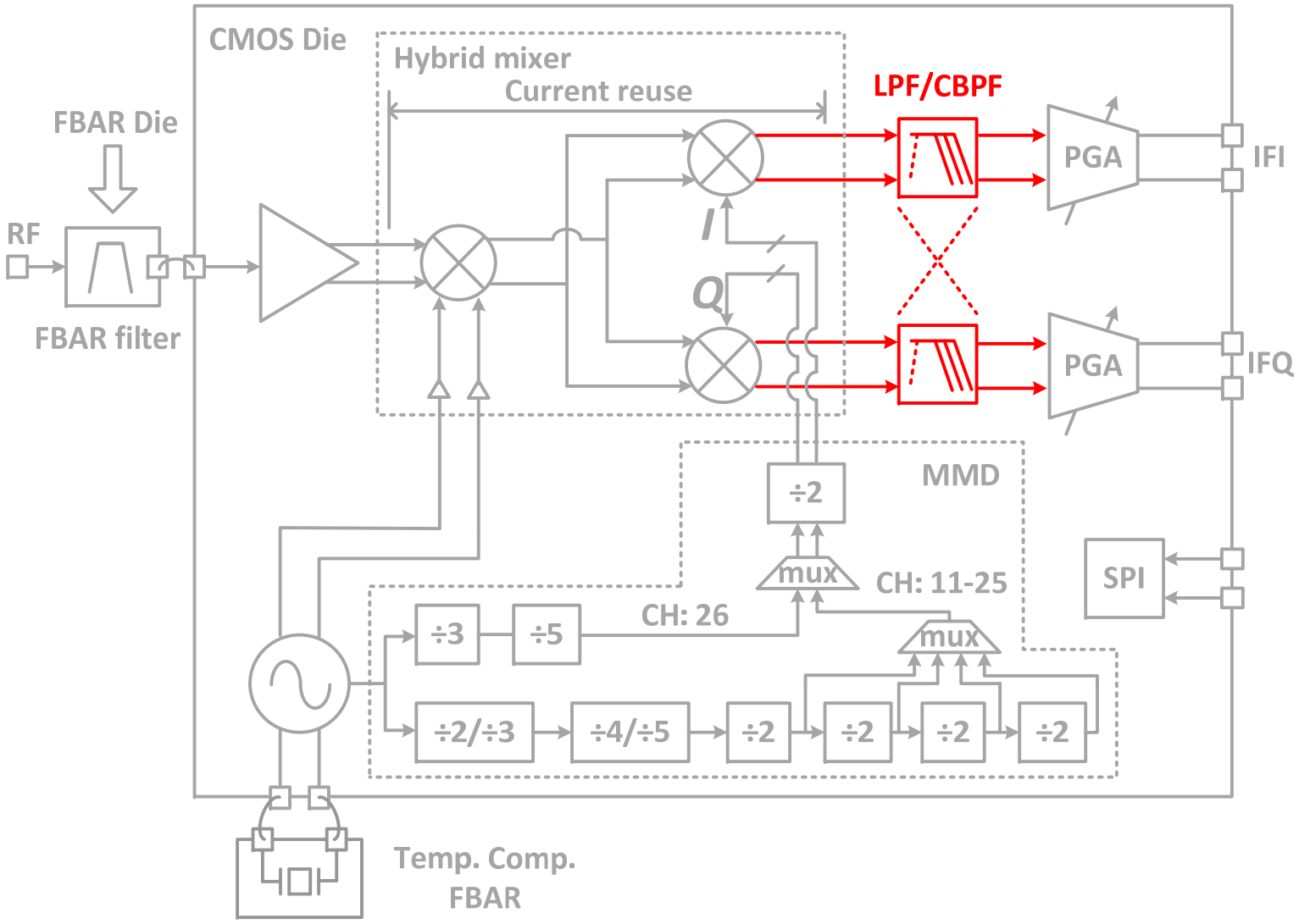
$Q_{parallel}$	Q_{series}	Q_{max}	$\|Z\|_{max}$
1348	1024	1496	>2 kΩ

FBAR Temperature Coefficient

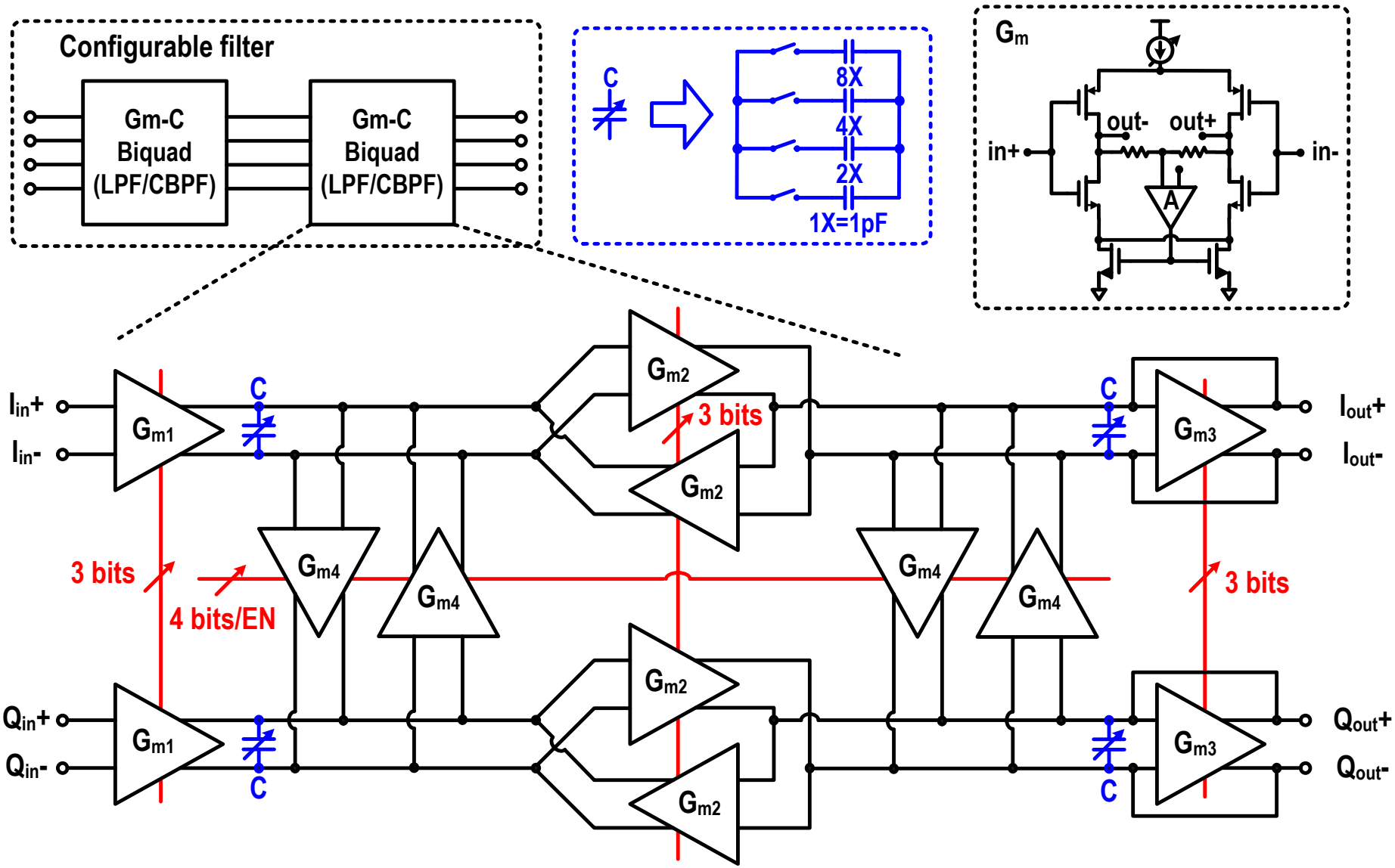


- The frequency dependence on temperature is quadratic with a coefficient of ~ -16 PPB/C^2.
- There is a 3rd order term that creates +/-5 ppm deviation on the quadratic.
- Typical Over-Temperature performance: +/- 50 ppm from -40°C to 100°C.

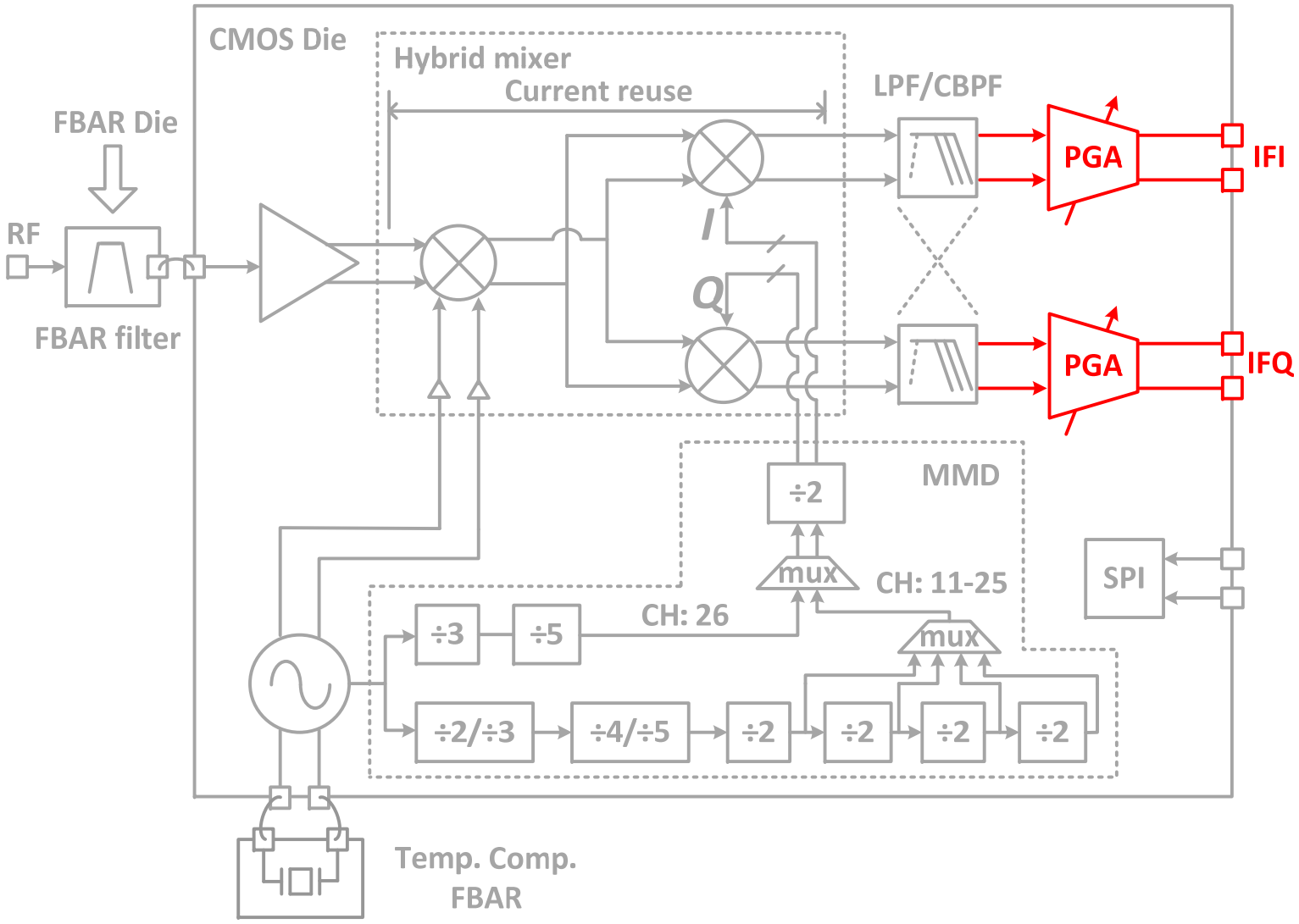
Proposed Filter



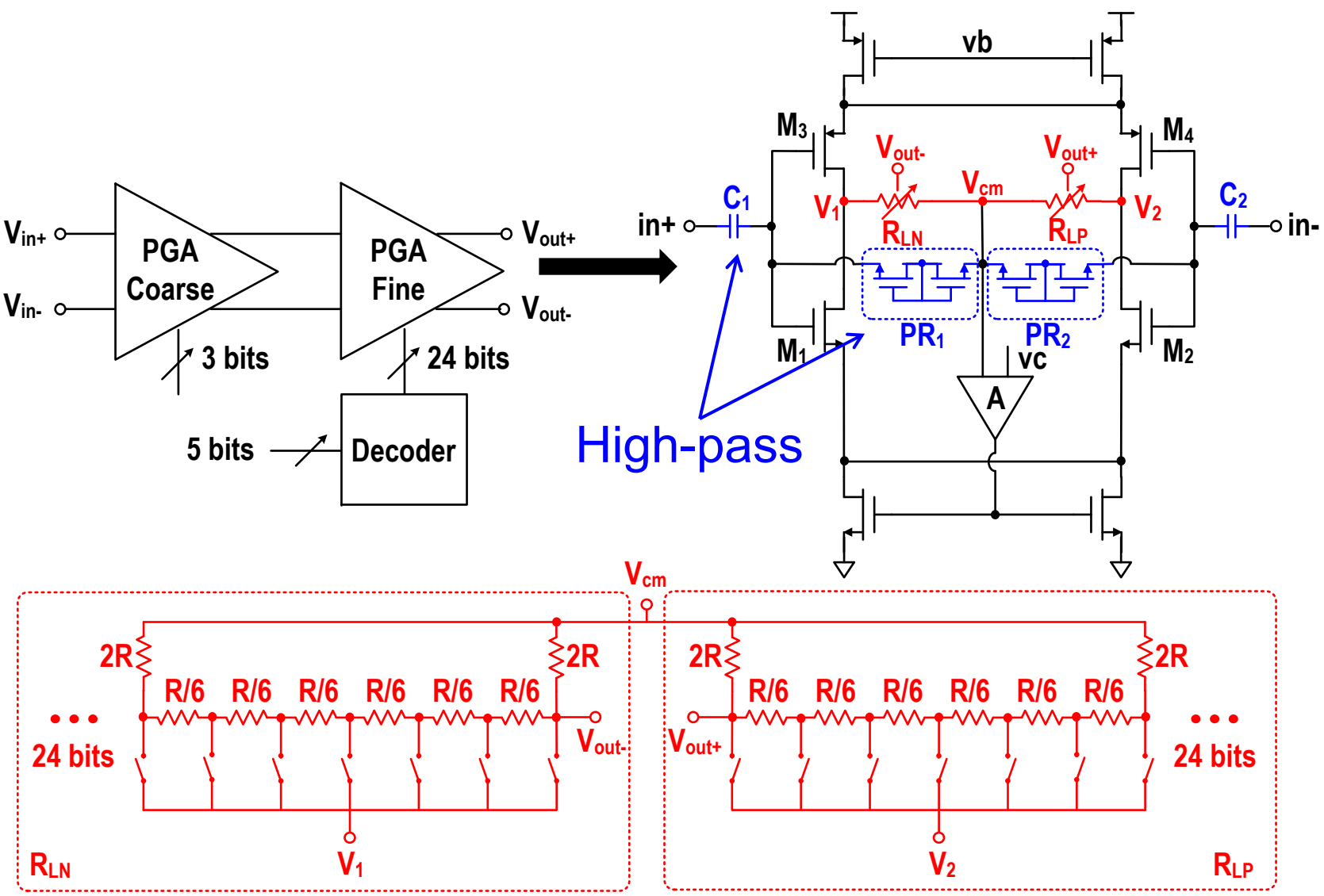
Filter Block Diagram



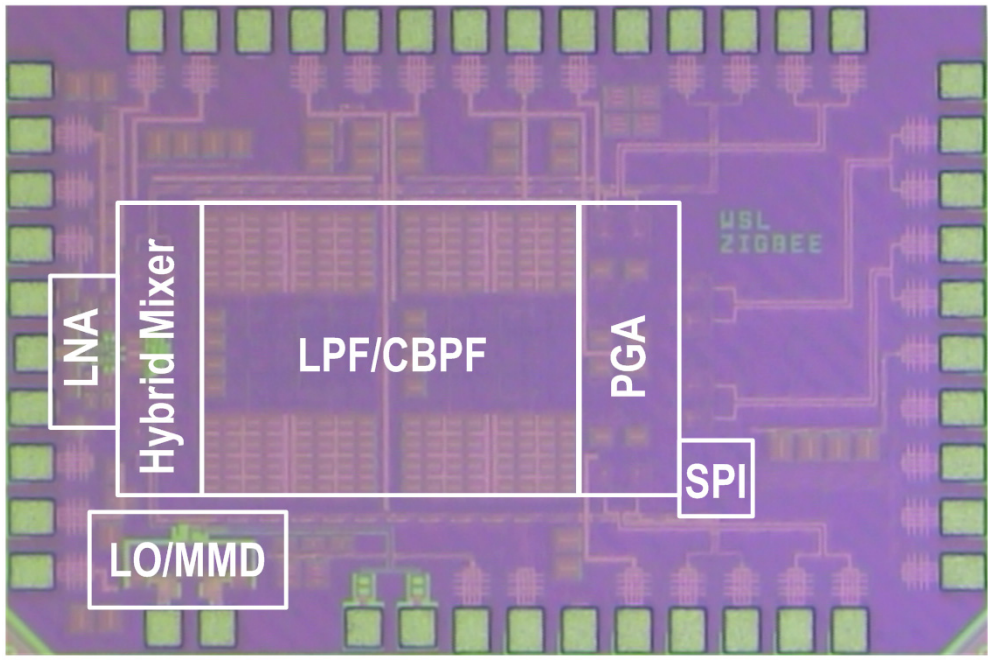
Proposed PGA



PGA Block Diagram

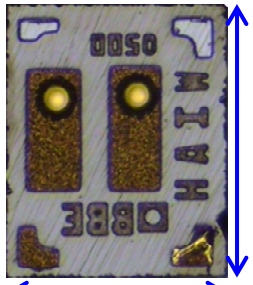


Die Photo

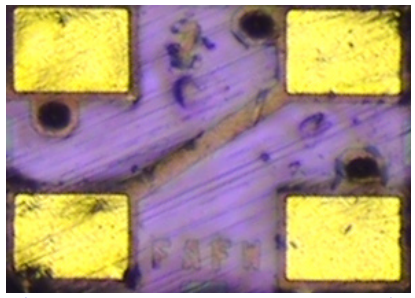


TSMC 65-nm CMOS

Core active area: 0.45mm²

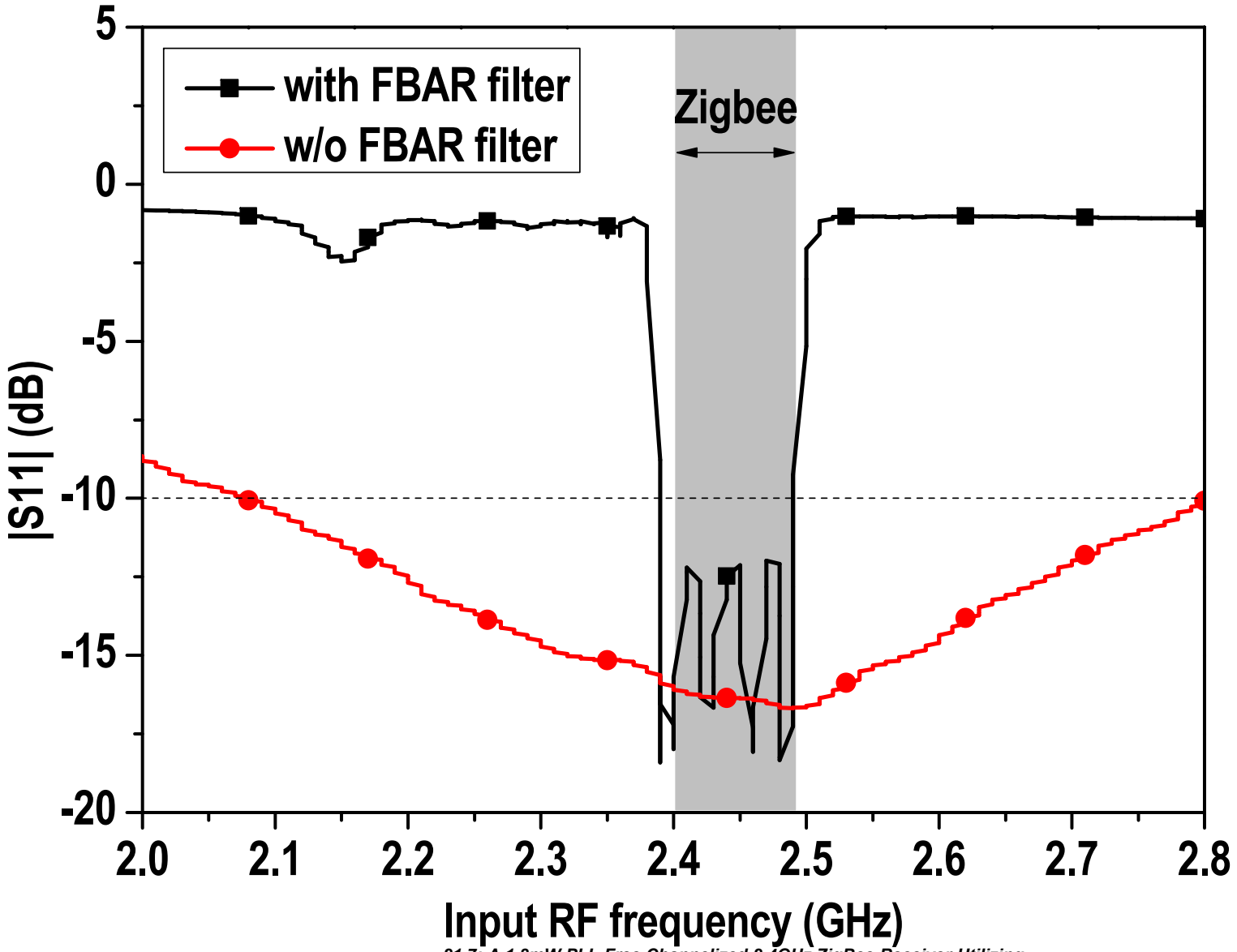


Temp. Comp. FBAR

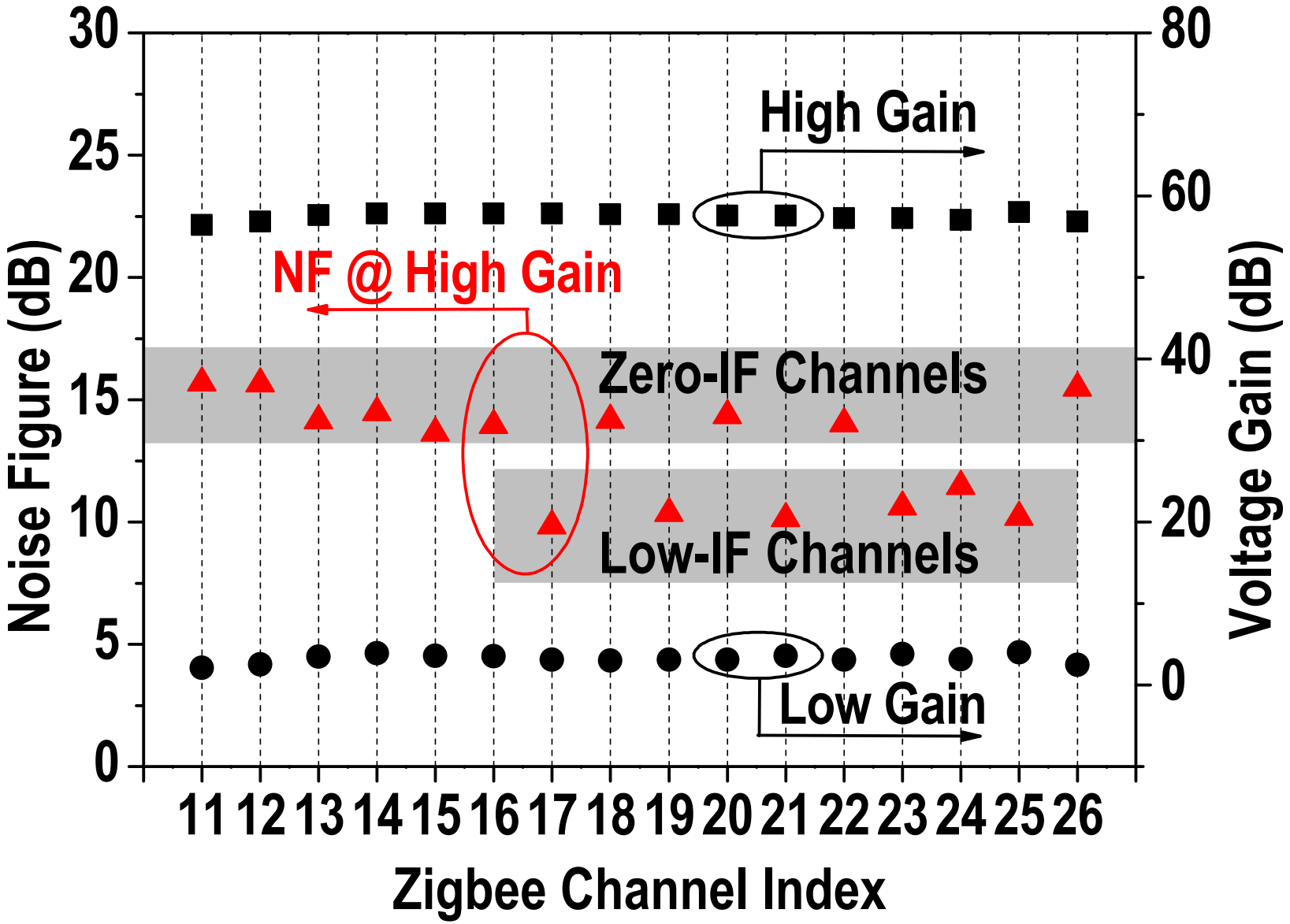


FBAR Filter

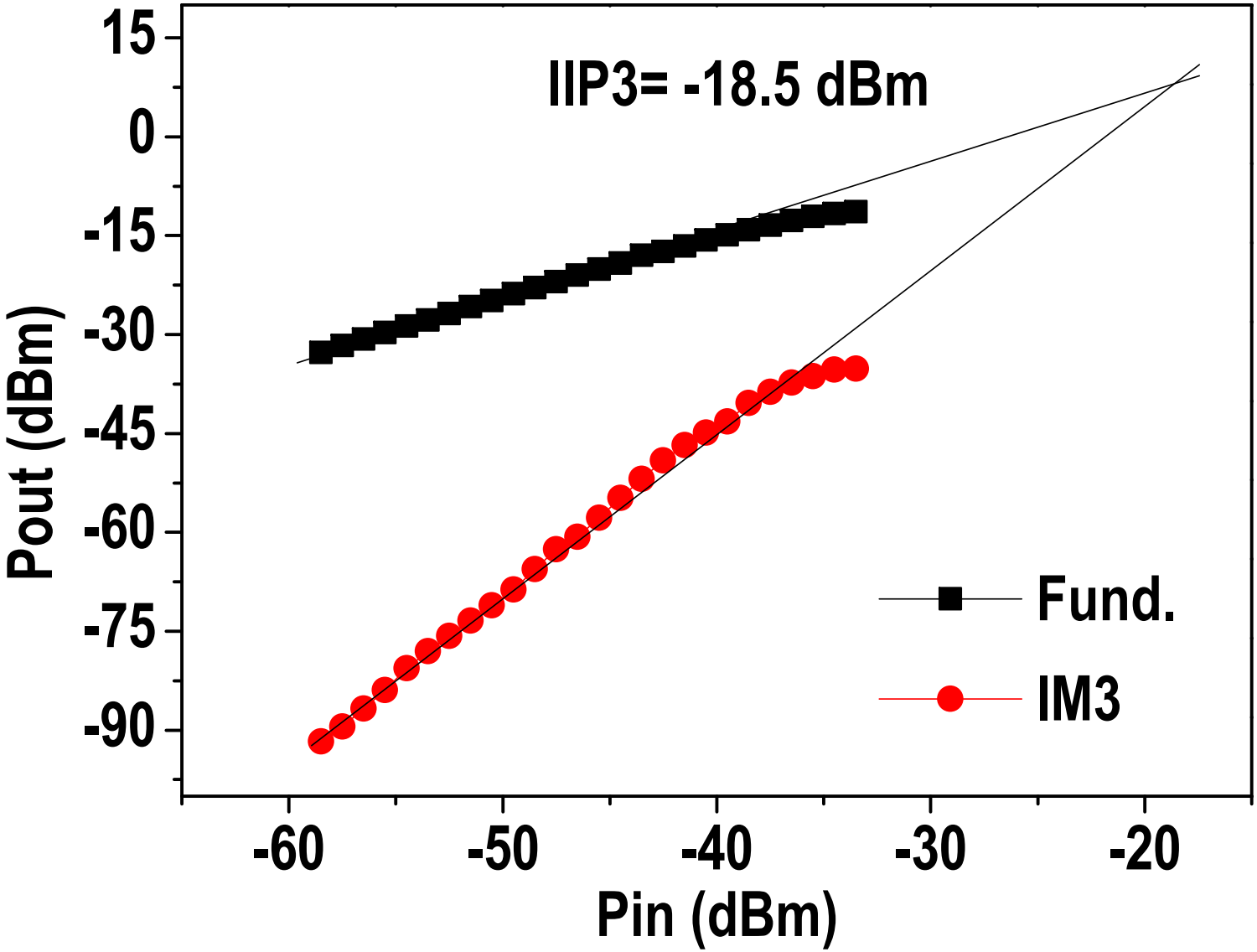
Measured |S11|



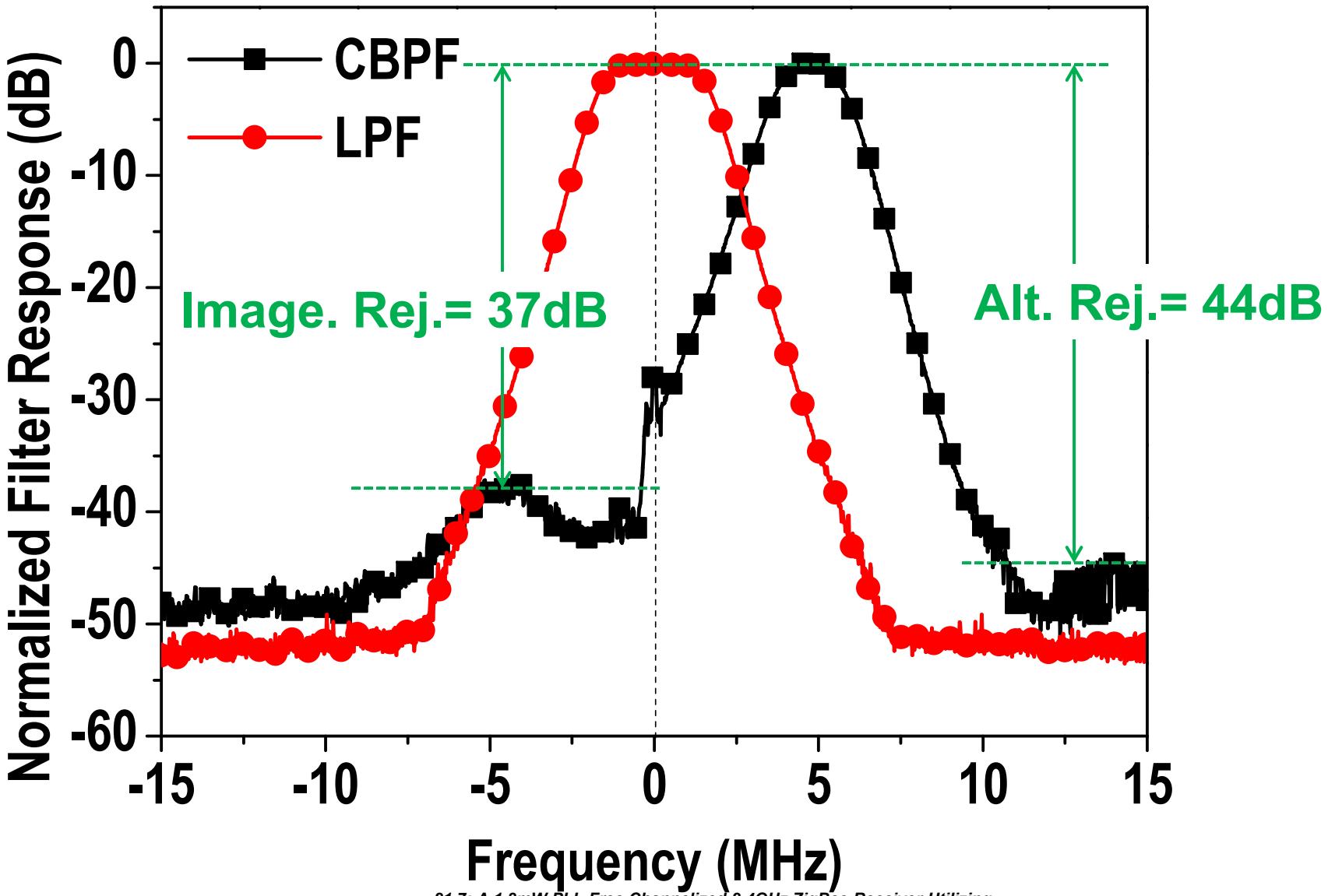
Measured Gain & NF



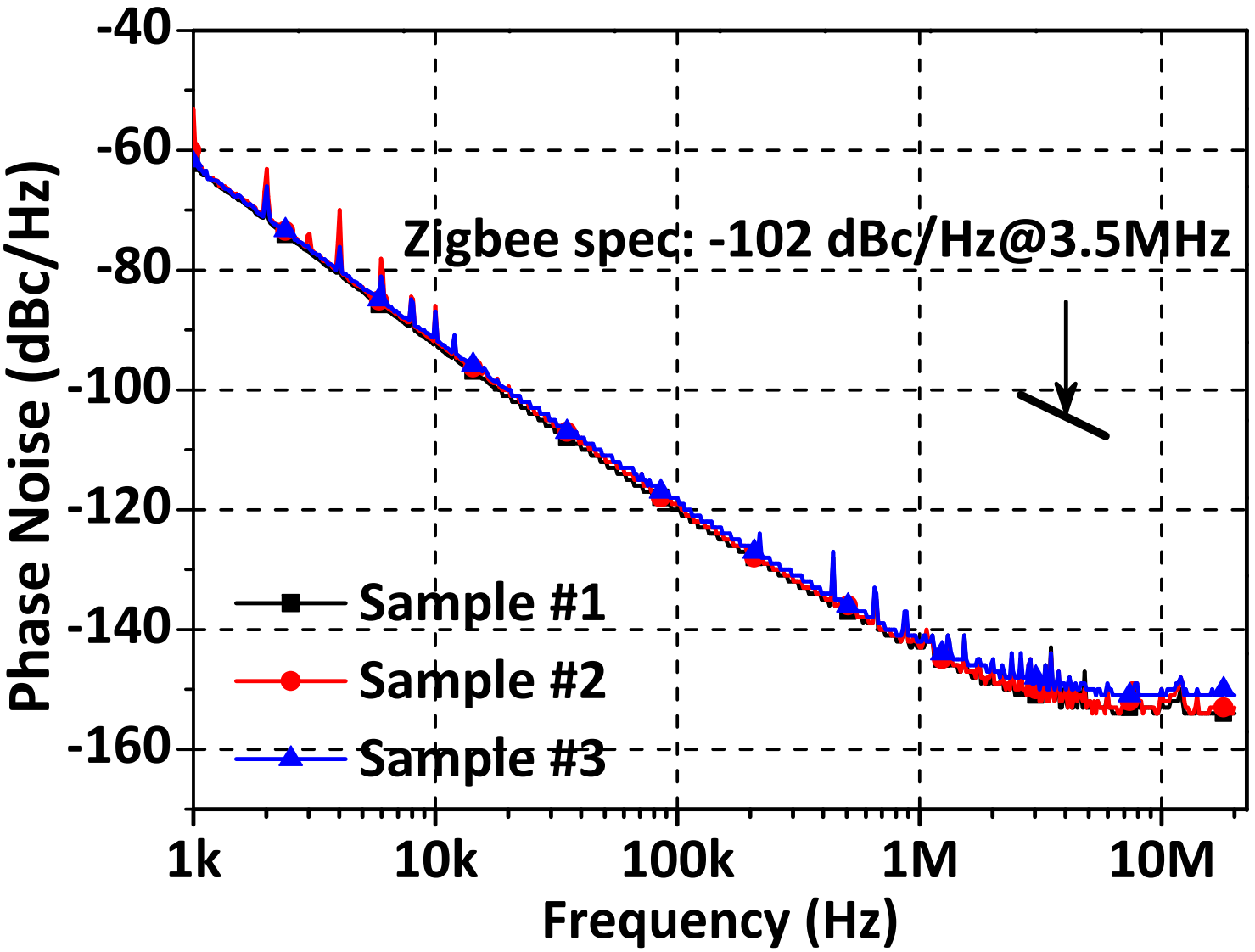
Measured IIP3



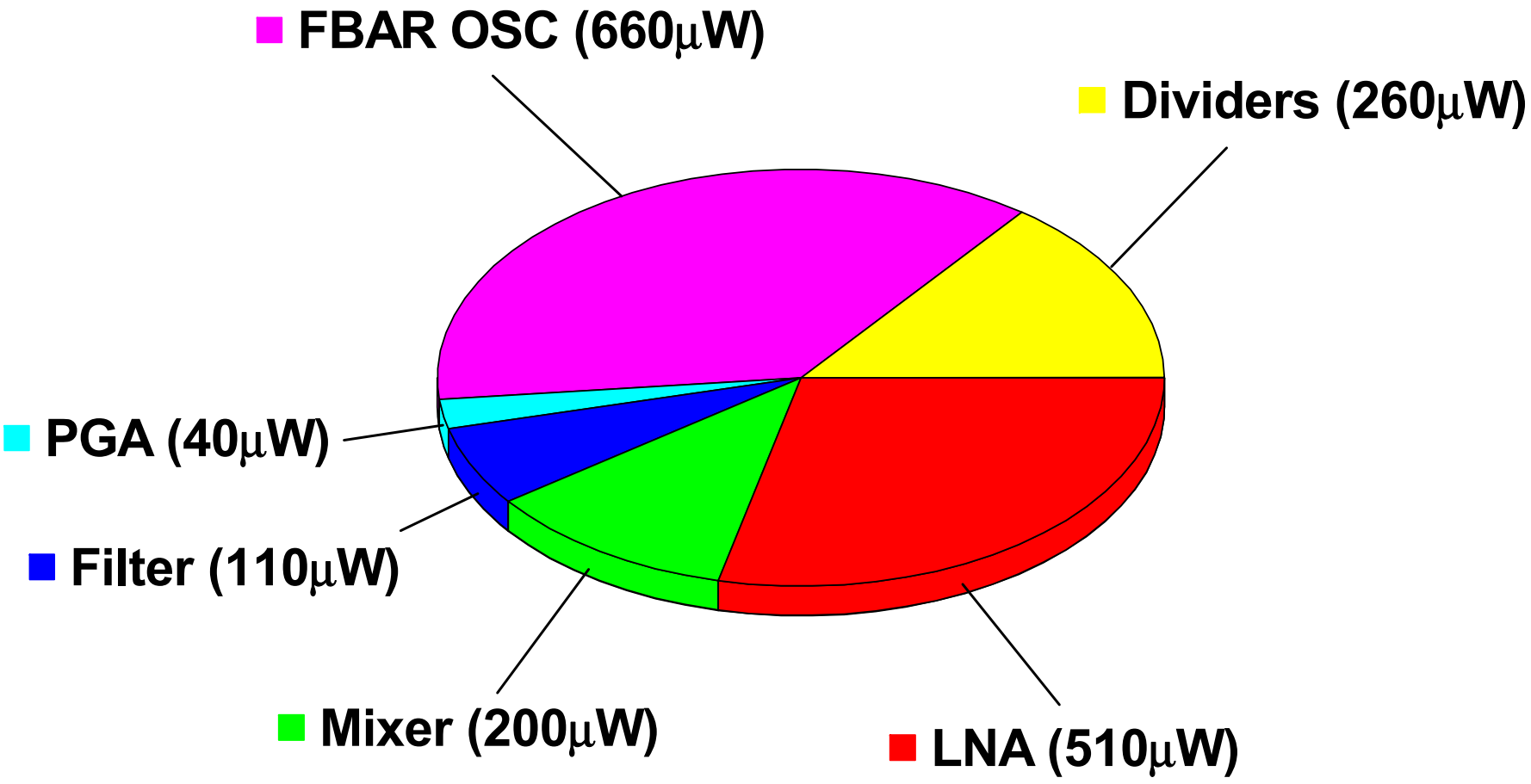
Measured Filter Response



Measured Phase Noise



Power Breakdown



- Total power consumption: 1.8 mW @ 1V

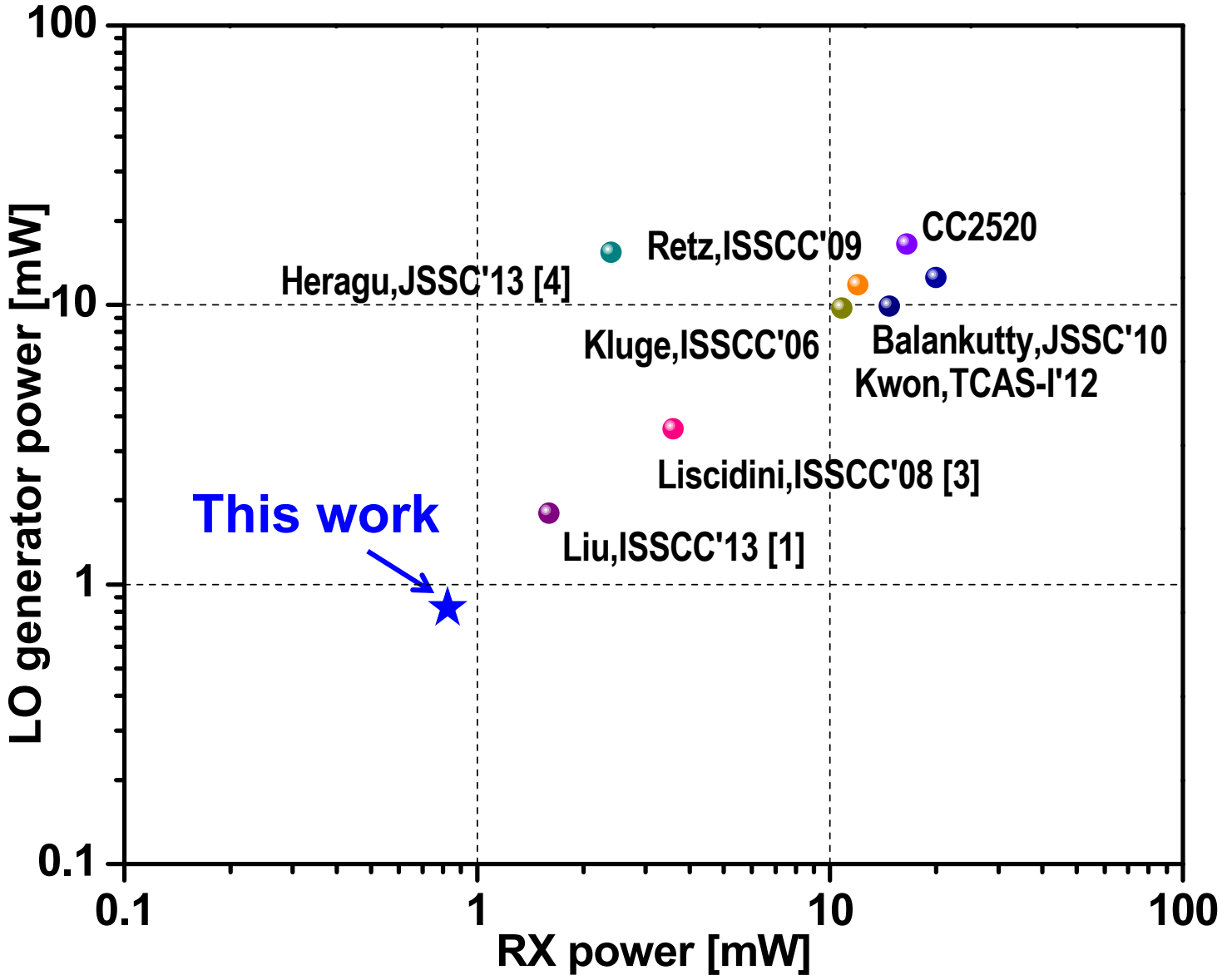
Performance Comparison (1)

	This work	ISSCC 2013 [1]	ISSCC 2008 [3]	JSSC 2013 [4]	ISSCC 2013 [5]	JSSC 2010 [8]
Standard	Zigbee	Zigbee/BT/ MBAN	Zigbee	N/A	Zigbee	Zigbee/BT
Architecture	Sliding-IF RX+LO	Sliding-IF RX+TX+PLL	Low-IF RX	Sliding-IF RX+PLL	Low-IF RX	Low-IF/ Zero-IF RX+PLL
XTAL	No	Yes	N/A	No	N/A	Yes
PLL-free	**Yes**	No	No	No	No	No
On-chip Inductors	**No**	Yes	Yes	Yes	Yes	Yes

Performance Comparison (2)

	This work	ISSCC 2013 [1]	ISSCC 2008 [3]	JSSC 2013 [4]	ISSCC 2013 [5]	JSSC 2010 [8]
Supply [V]	1	1.2	1.2	1.8	0.6/1.2	0.6
RX Power [mW]	**0.86**	>1.6	3.6	2.4	1.7	20
LO Power [mW]	**0.92**	1.8	N/A	15.4	N/A	12.5
Gain [dB]	57.8	N/A	75	44.2	57	67
NF [dB]	15.7	6	12	14.8	8.5	16
IIP_3 [dBm]	-18.5	-19	-12.5	-28	-6	-10.5
Image-rejection [dB]	**1^{st} = 40dB 2^{nd} = 37dB**	35	35	N/A	36	32
PN @ 3.5MHz [dBc/Hz]	**-144**	N/A	-107	N/A	N/A	-127
Technology	65-nm	90-nm	90-nm	180-nm	65-nm	90-nm
Active Area [mm^2]	0.45	2	0.35	N/A	0.22	1.45

Performance Comparison (3)



Conclusion

- A 2.4GHz ZigBee receiver with a fixed-LO frequency plan utilizing a temp-compensated FBAR has been presented.
- The PLL is eliminated by directly dividing down the fixed FBAR oscillator frequency.
- Demonstrates **2X** improvement in receiver power consumption.
- Demonstrates **17dB** improvement in LO phase noise.

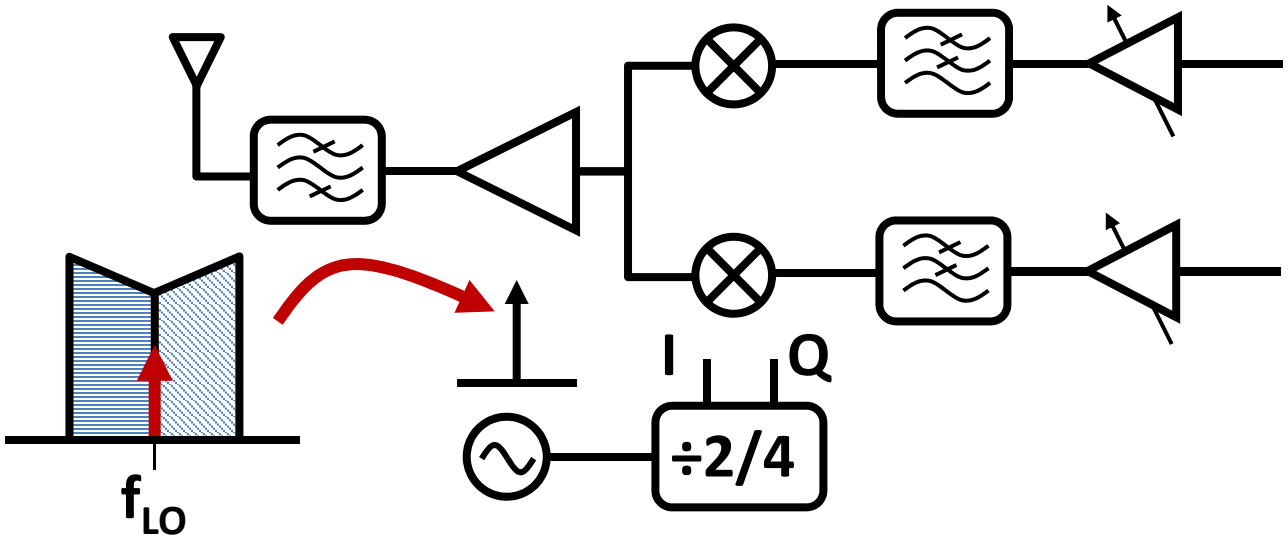
Pulling Mitigation in Wireless Transmitters

A. Mirzaei, M. Mikhemar, H. Darabi

Broadcom Corporation

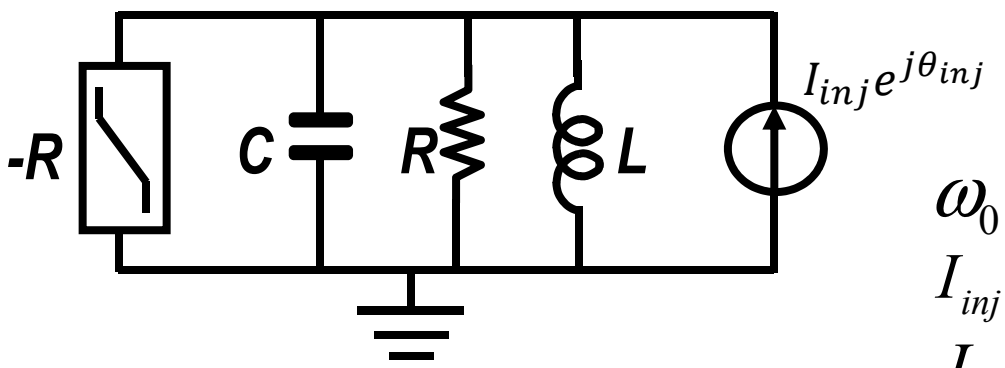
February 2014

Motivation



- Direct-conversion transmitter: low power, versatile
- But suffers from pulling
  - May require revisions to mitigate in 2G/3G/4G applications
  - Not used in applications such as WLAN or BT with on-chip PAs
- Multiple close-by VCO's on chip due to FDD, CA, …

Free-Running LC Oscillator Under Injection



$$\frac{d\theta}{dt} = \omega_0 + \frac{\omega_0}{2Q}\frac{I_{inj}\sin(\theta_{inj}-\theta)}{I_S + I_{inj}\cos(\theta_{inj}-\theta)}$$

ω_0 : **free-running frequency**

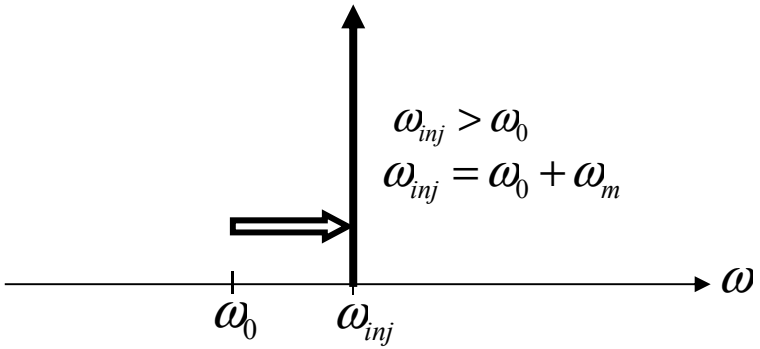
I_{inj} : **magnitude of injection current**

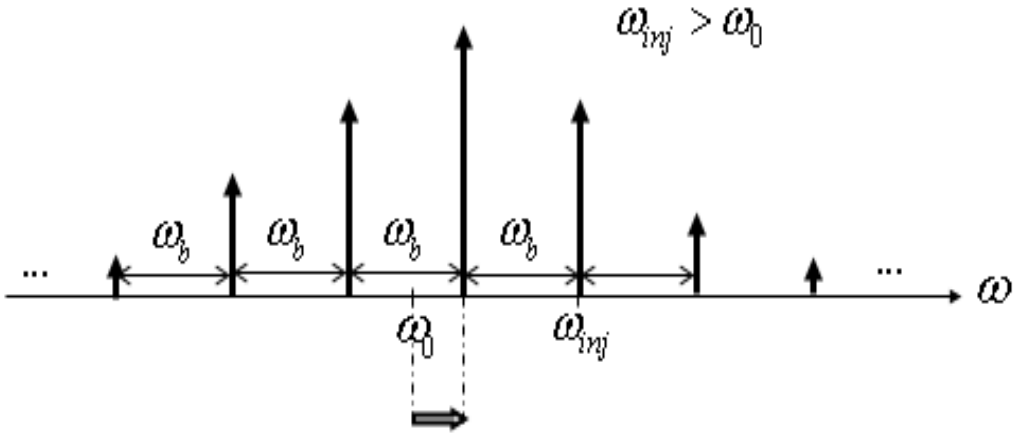
I_S : **magnitude of signal current**

pulling strength: $\eta = \frac{I_{inj}}{I_S}\sqrt{1+\left(\frac{\omega_0}{2Q}\frac{1}{\omega_{inj}-\omega_0}\right)^2}$

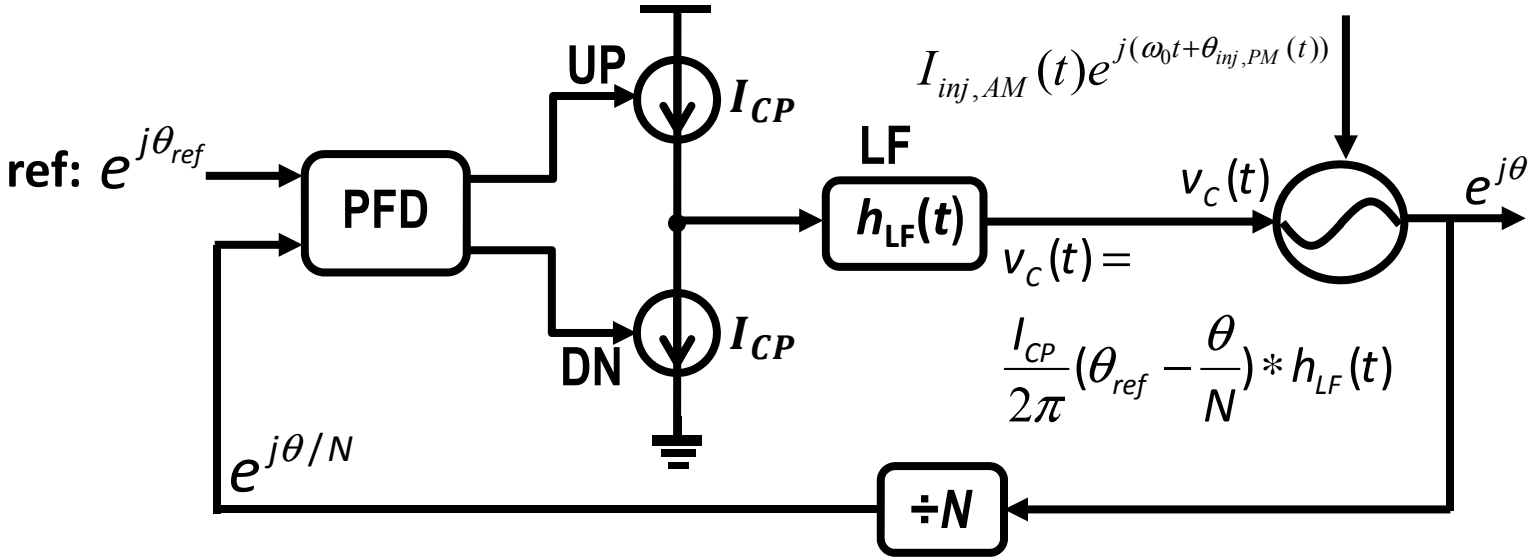
$\eta > 1$: *locking*

$\eta < 1$: *pulling*





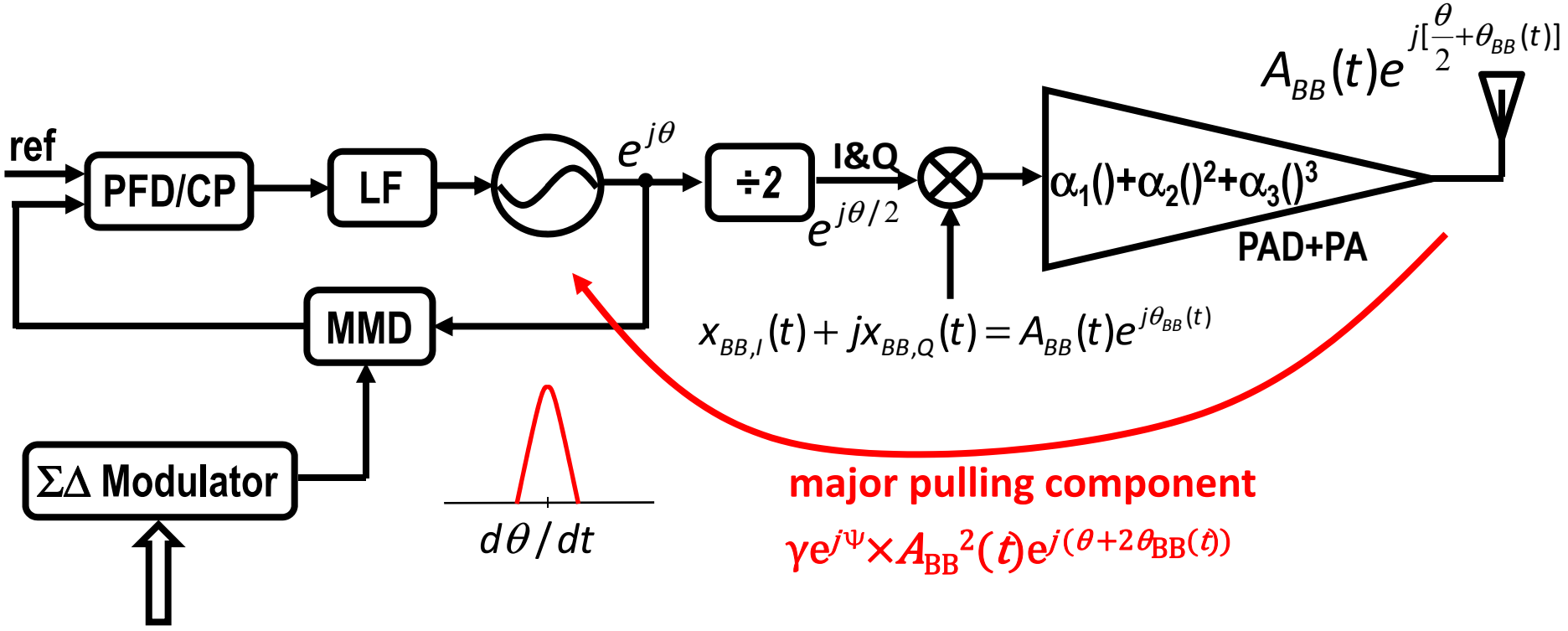
Locked Oscillator Pulled by Modulated Signal



- **Differential equation for VCO phase:**

$$\frac{d\theta}{dt}=K_{VCO}\frac{I_{CP}}{2\pi}(\theta_{ref}-\frac{\theta}{N})*h_{LF}(t)+\frac{\omega_0}{2Q}\frac{I_{inj,AM}(t)\sin(\omega_0 t+\theta_{inj,PM}(t)-\theta)}{I_S+I_{inj,AM}(t)\cos(\omega_0 t+\theta_{inj,PM}(t)-\theta)}$$

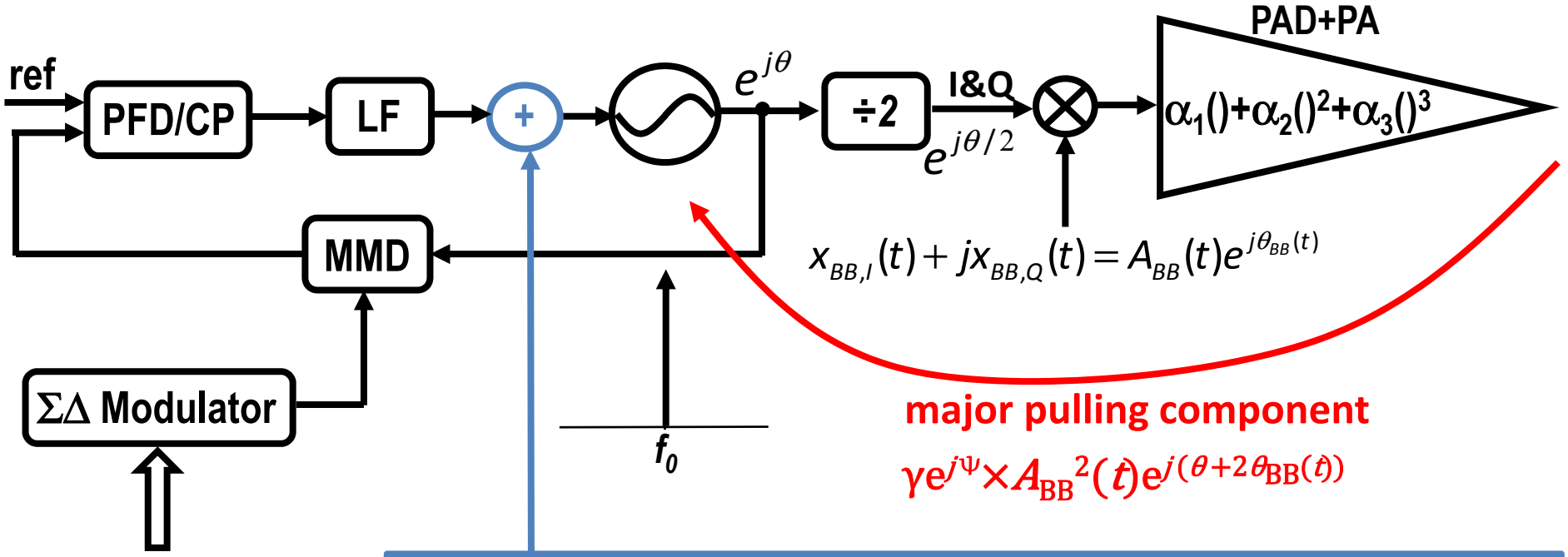
Locked Oscillator Pulled by Transmitter Signal



A low-frequency baseband signal, independent of θ

$$\frac{d\theta}{dt}=K_{VCO}\frac{I_{CP}}{2\pi}(\theta_{ref}-\frac{\theta}{N})*h_{LF}(t)+\frac{\omega_0}{2Q}\frac{\gamma A_{BB}^2(t)\sin(2\theta_{BB}(t)+\psi)}{I_S+\gamma A_{BB}^2(t)\cos(2\theta_{BB}(t)+\psi)}$$

Pulling Elimination by Modifying Control Voltage

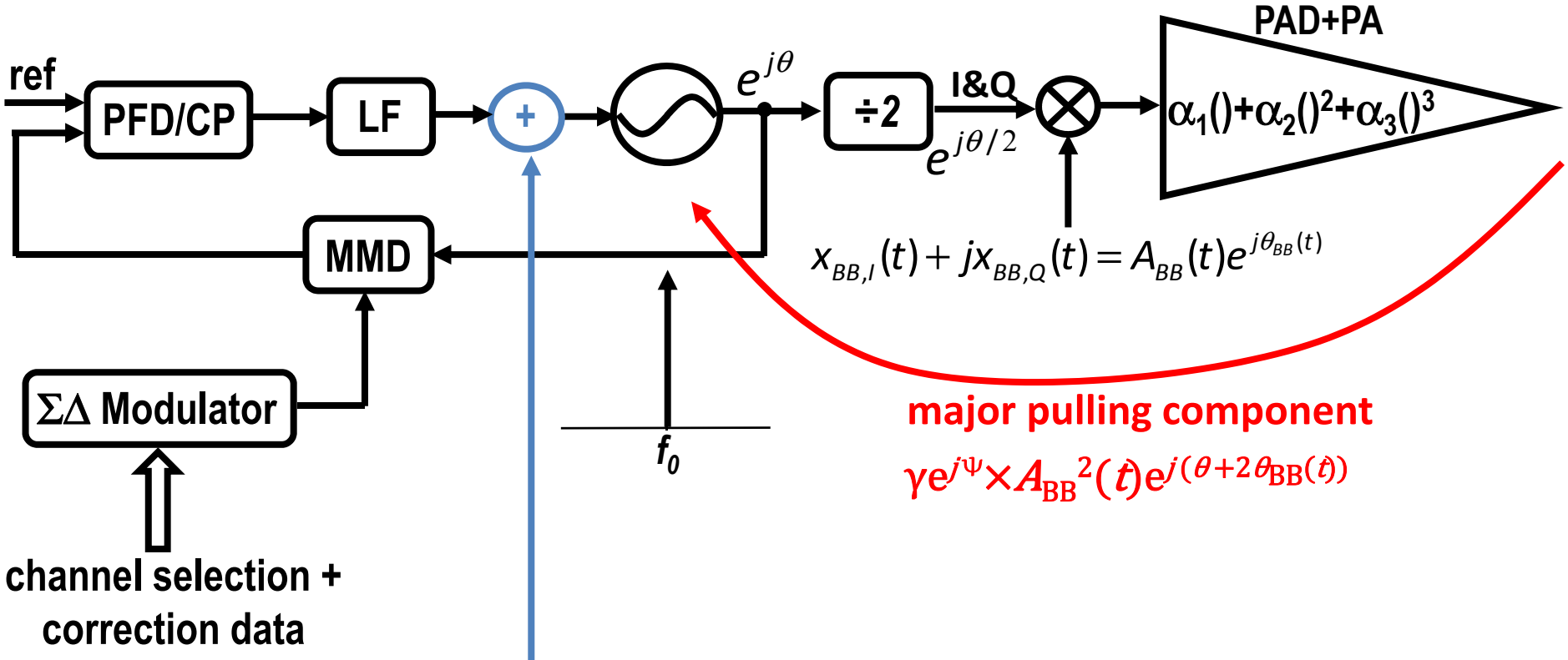


$$v_{correction}(t) = -\frac{1}{K_{VCO}} \frac{\omega_0}{2Q} \frac{\gamma A_{BB}^2(t)\sin(2\theta_{BB}(t)+\psi)}{I_S + \gamma A_{BB}^2(t)\cos(2\theta_{BB}(t)+\psi)}$$

$$A_{BB}^2(t)\sin(2\theta_{BB}(t)) = 2x_{BB,I}(t).x_{BB,Q}(t)$$

$$A_{BB}^2(t)\cos(2\theta_{BB}(t)) = x_{BB,I}^2(t) - x_{BB,Q}^2(t)$$

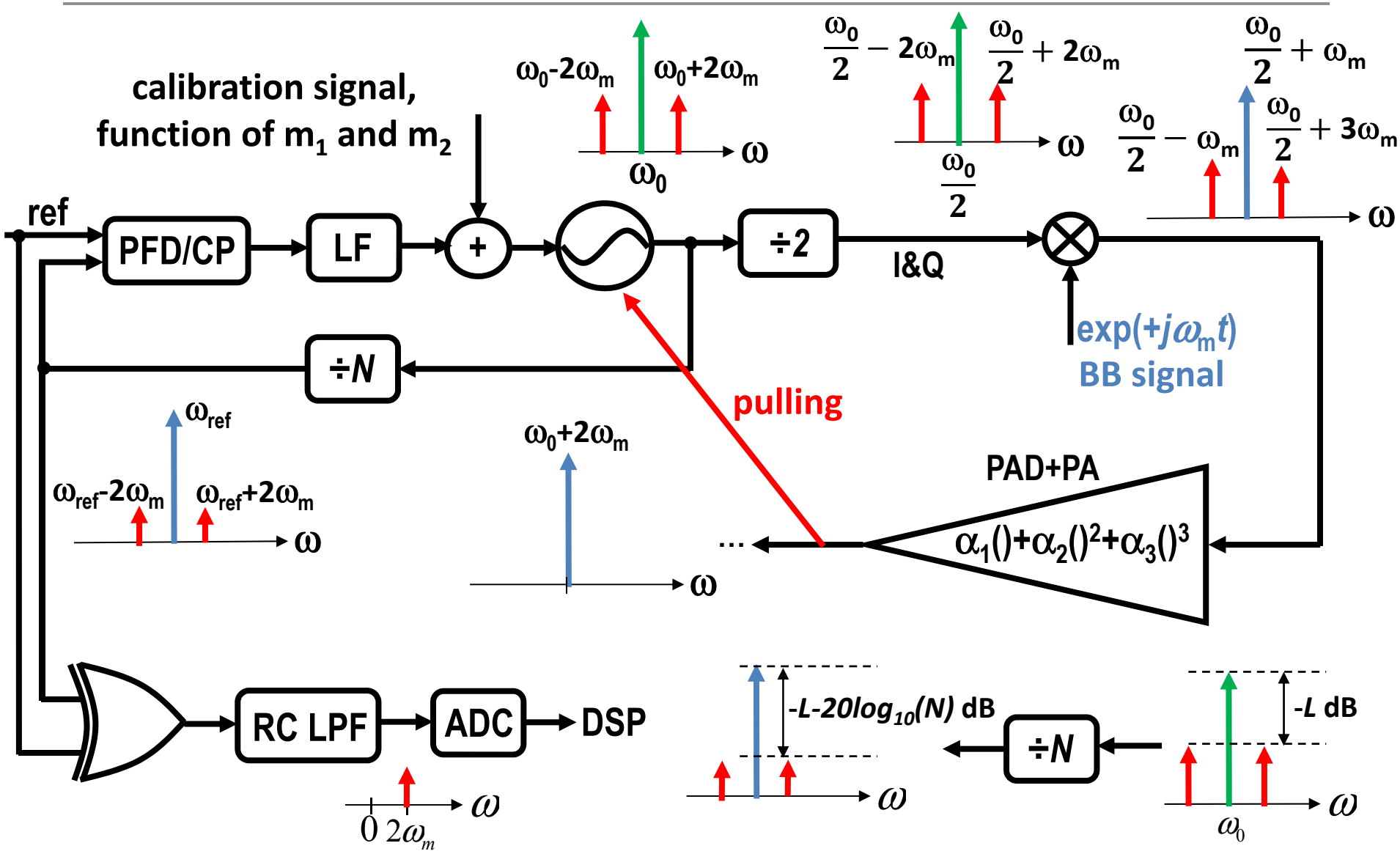
Pulling Elimination by Modifying Control Voltage



$$v_{correction}(t)=-\frac{1}{K_{VCO}}\frac{\omega_0}{2Q}\frac{m_1(x_{BB,I}^2(t)-x_{BB,Q}^2(t))+m_2(2x_{BB,I}(t)x_{BB,Q}(t))}{1+m_2(x_{BB,I}^2(t)-x_{BB,Q}^2(t))-m_1(2x_{BB,I}(t)x_{BB,Q}(t))}$$

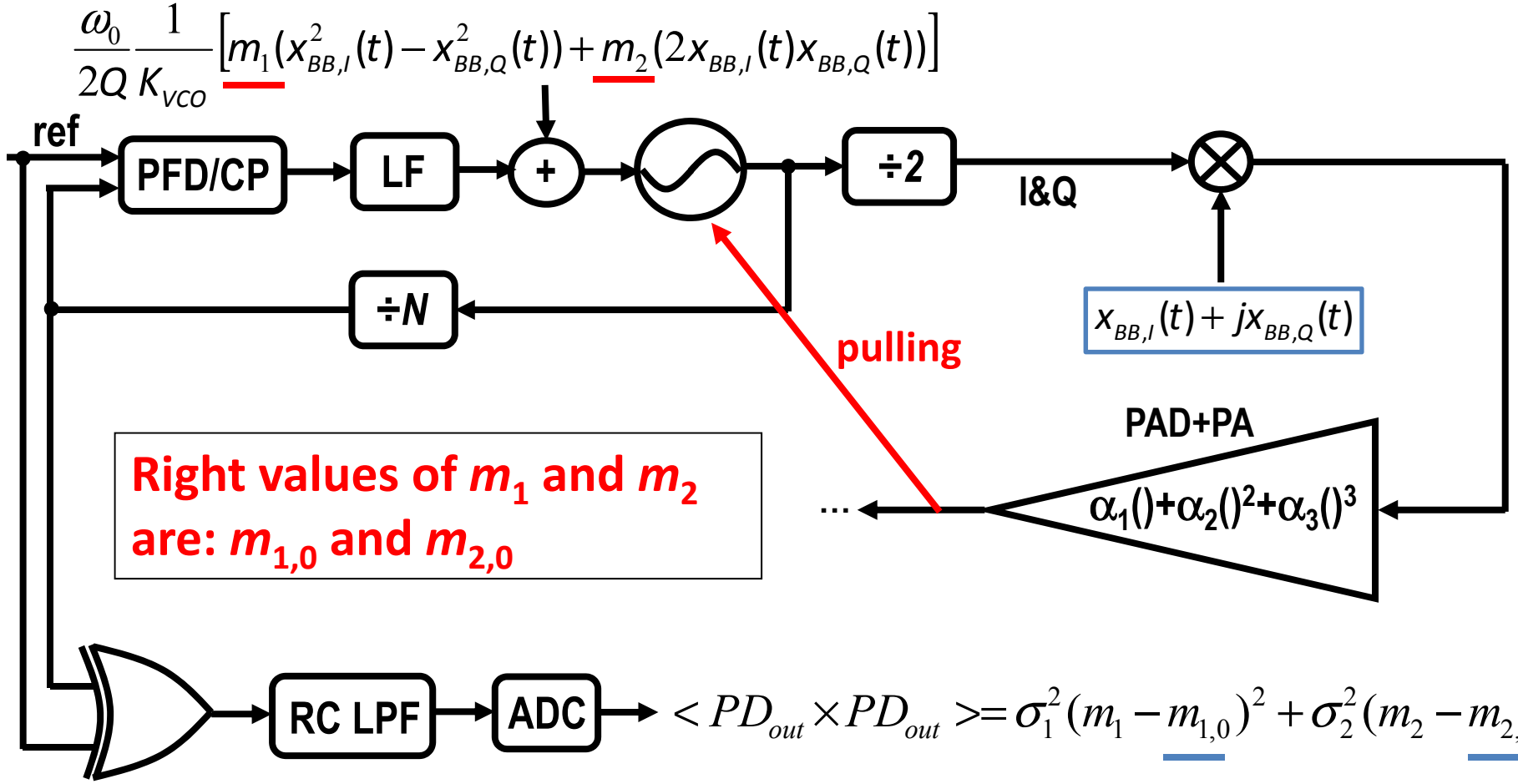
$m_1=\frac{\gamma\sin\psi}{I_S}$ & $m_2=\frac{\gamma\cos\psi}{I_S}$, m_1 and m_2 are found through calibration

TX-VCO Calibration with Tone



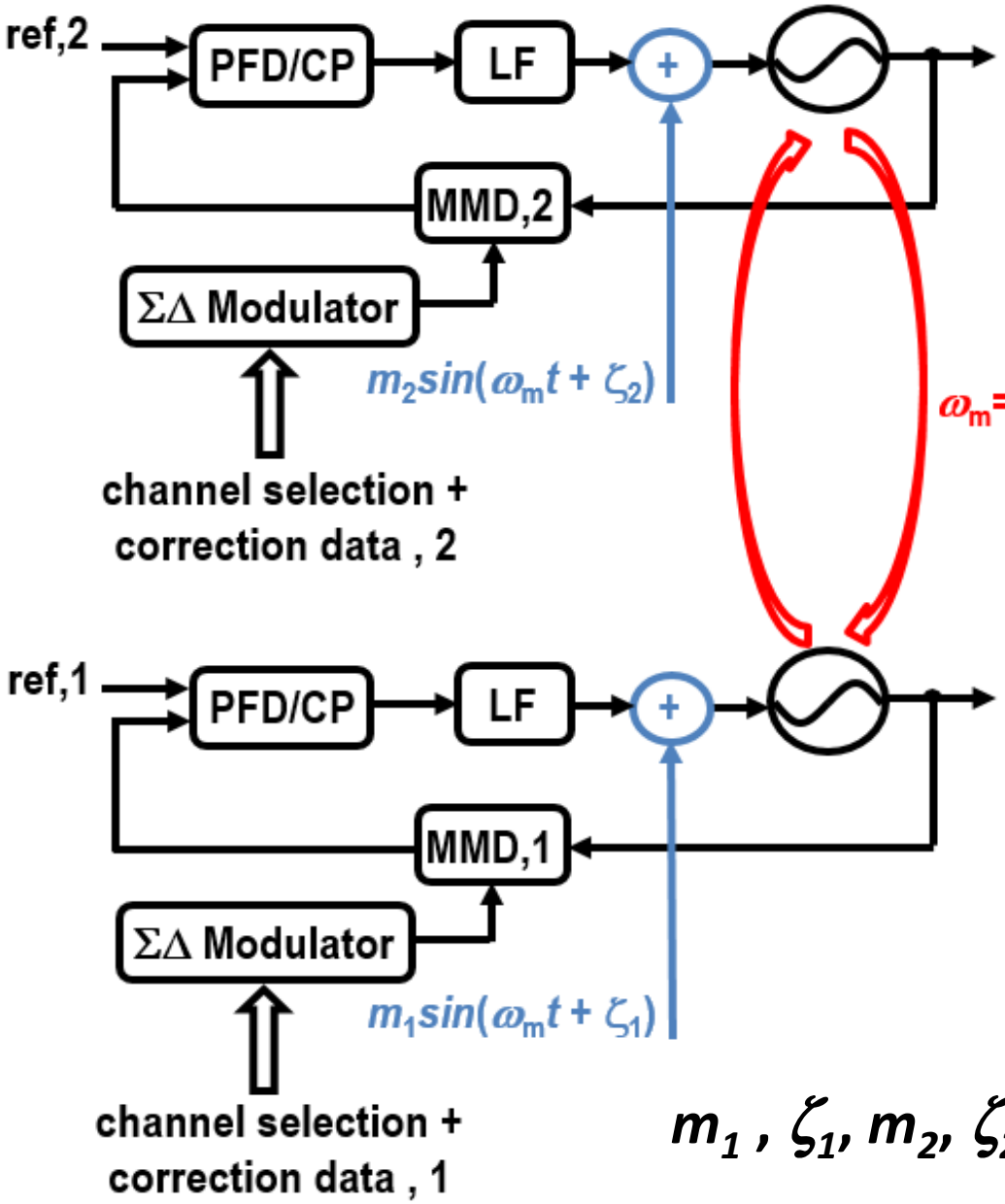
After calibration this tone disappears.

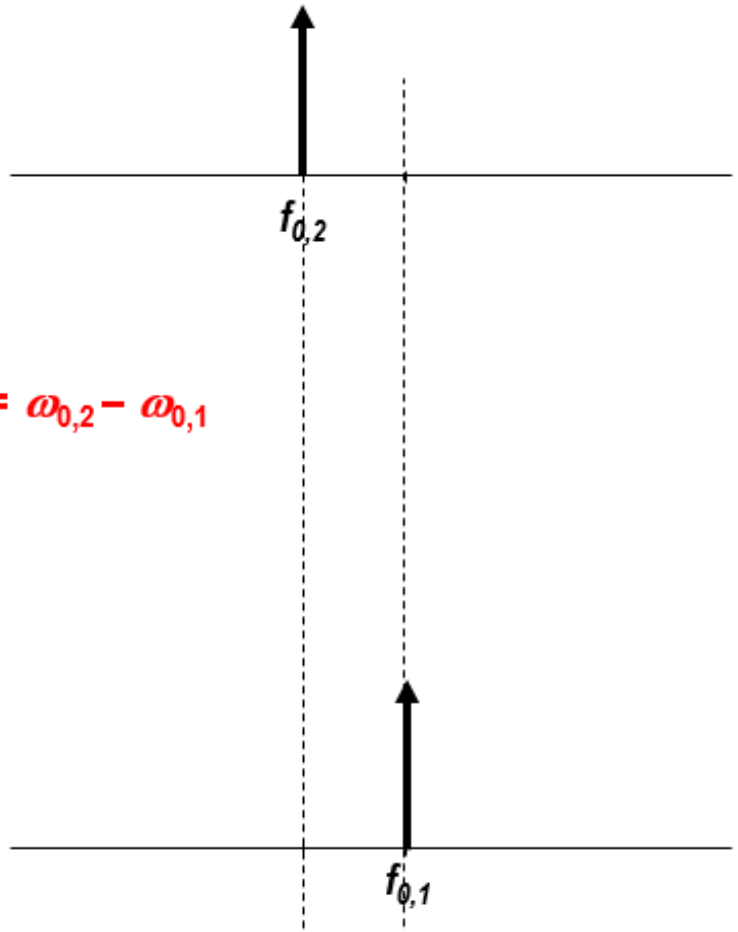
TX-VCO Real-Time Calibration



- $\sigma_{1/2}$ functions of BB signals & PLL, but independent of injection signal's strength and phase
- 2 simple 1D optimizations rather than 1 complicated 2D

Elimination of Mutual Pulling

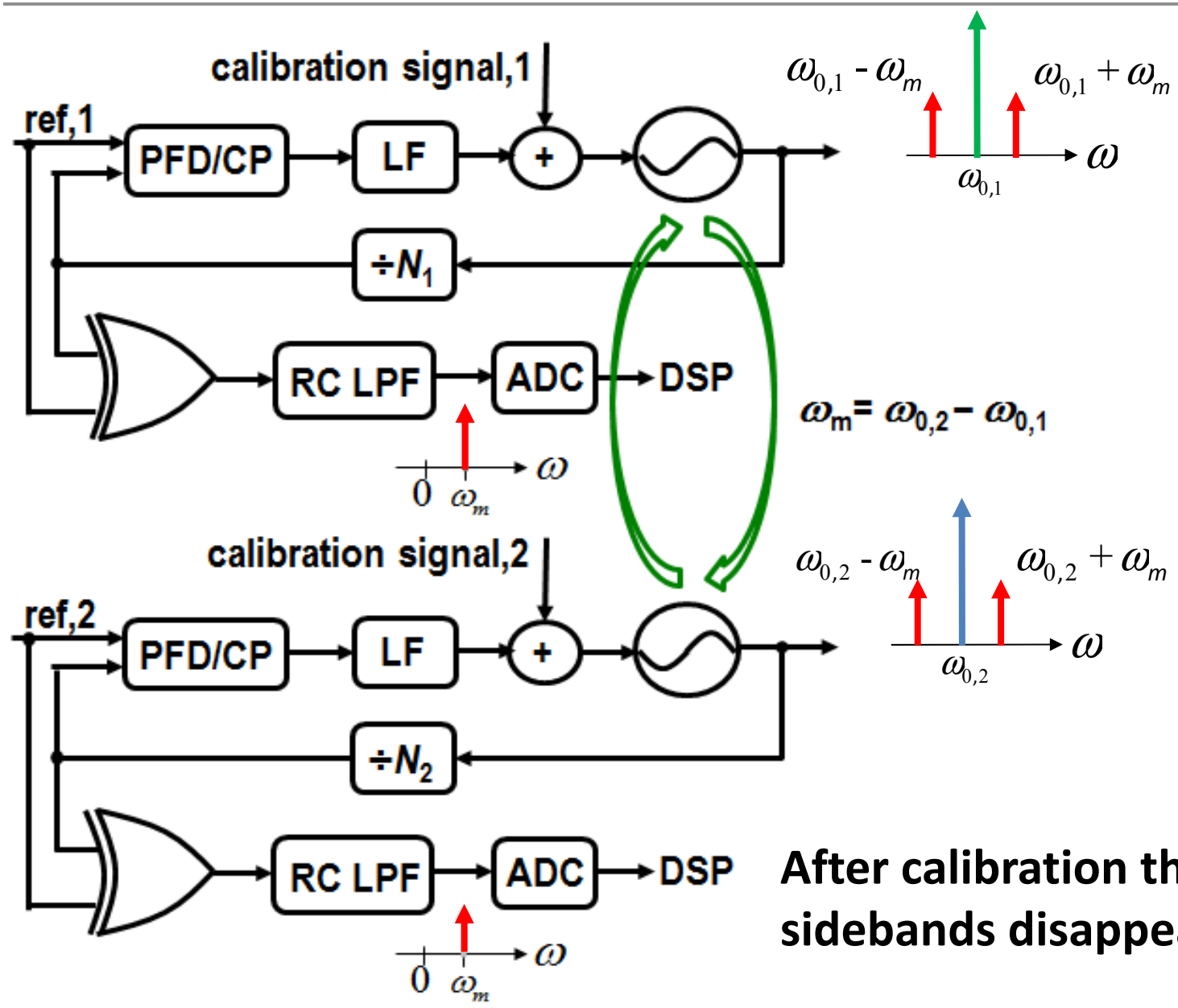




$\omega_m = \omega_{0,2} - \omega_{0,1}$

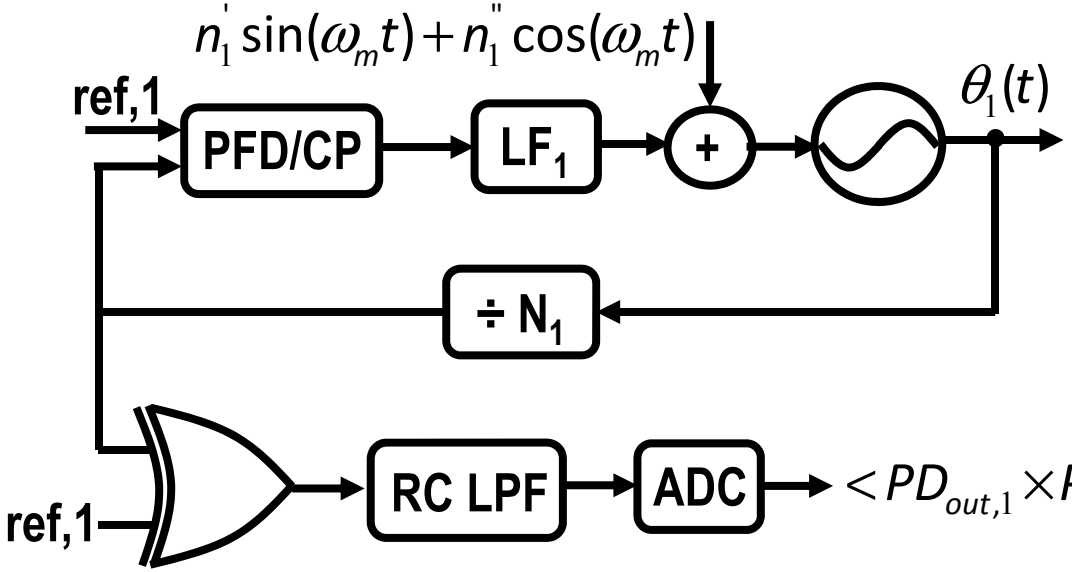
m_1 , ζ_1, m_2, ζ_2, are found through calibration

Calibration for Elimination of Mutual Pulling



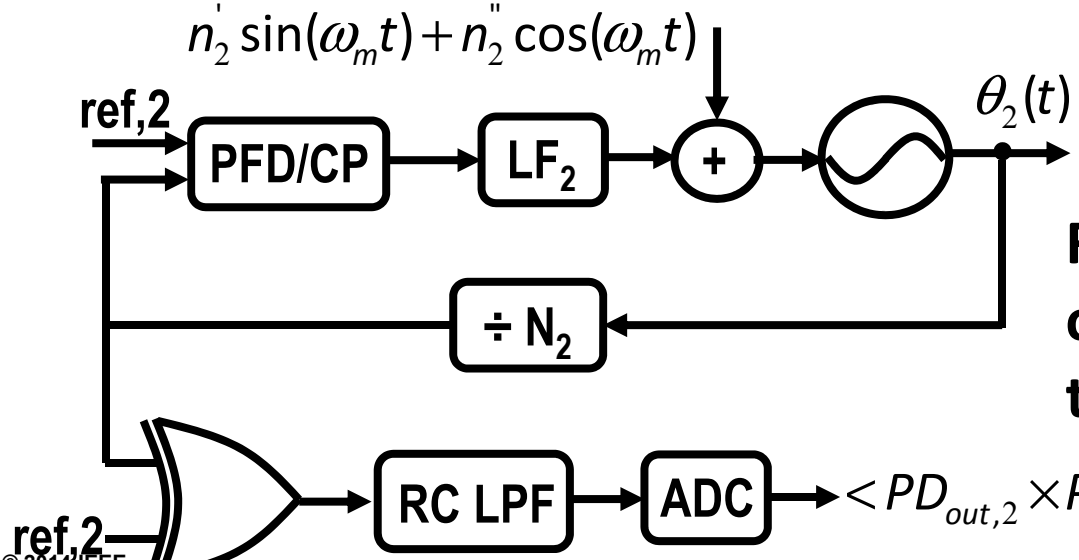
After calibration these two sidebands disappear.

Online calibration of Mutual Pulling



$$<PD_{out,1}\times PD_{out,1}>=\sigma_1^2(n_1^{'}-n_{1,0}^{'})^2+\sigma_1^2(n_1^{''}-n_{1,0}^{''})^2$$

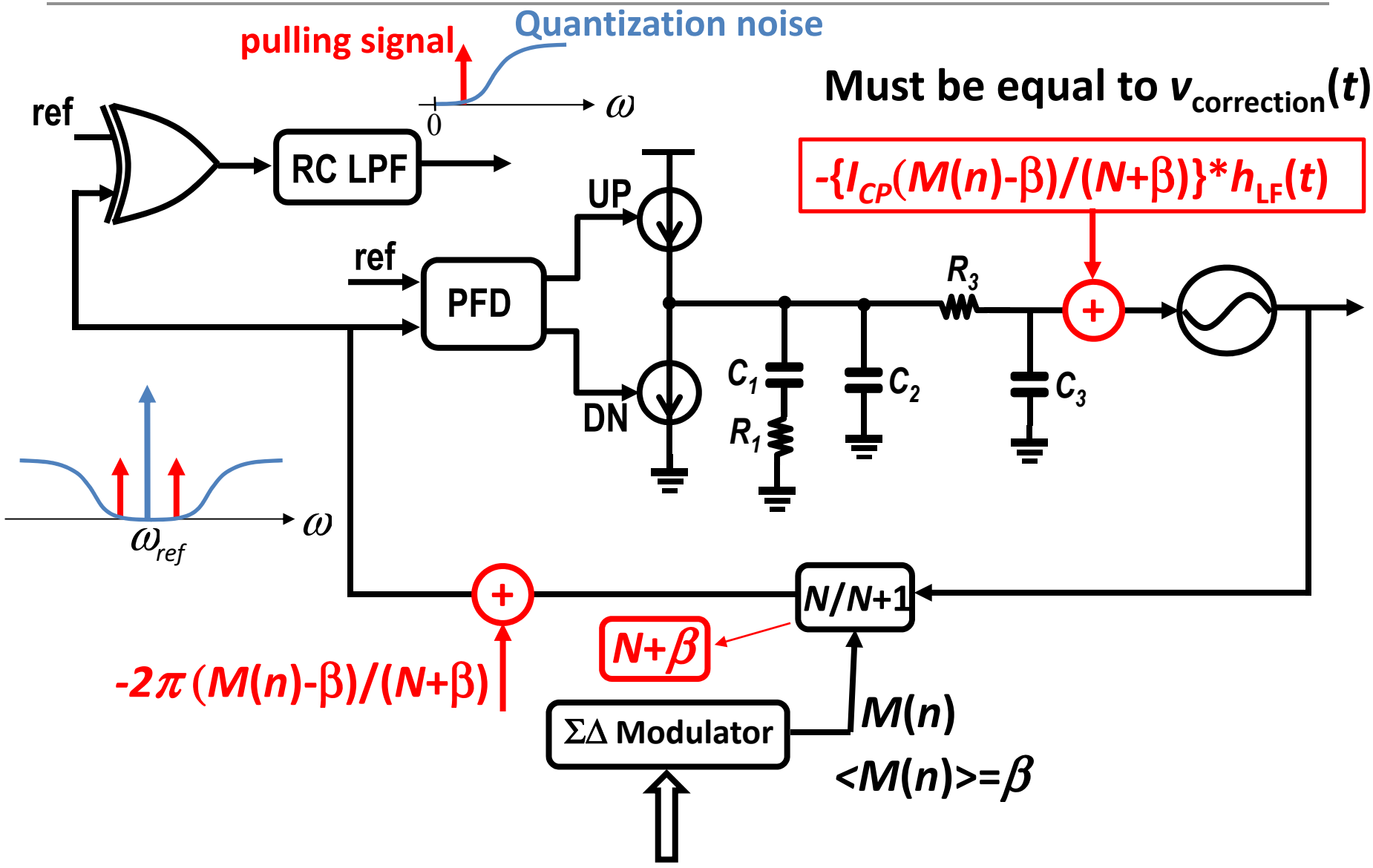
Right values of n'_1, n''_1, n'_2, and n''_2 are: $n'_{1,0}$, $n''_{1,0}$, $n'_{2,0}$, and $n''_{2,0}$



$$<PD_{out,2}\times PD_{out,2}>=\sigma_2^2(n_2^{'}-n_{2,0}^{'})^2+\sigma_2^2(n_2^{''}-n_{2,0}^{''})^2$$

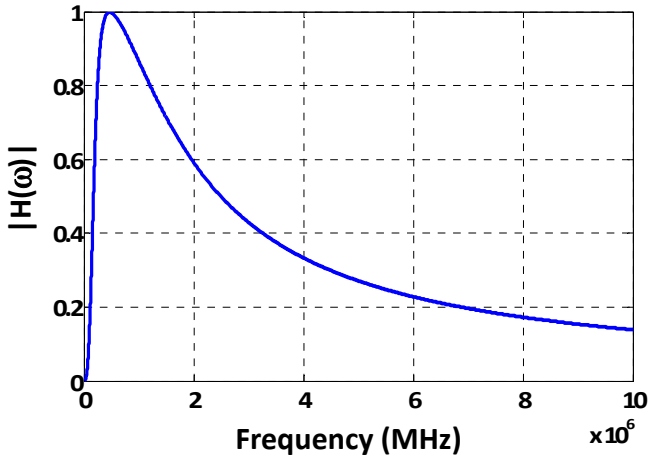
Four simple one-dimensional optimizations needed rather than one 4-dimensional one

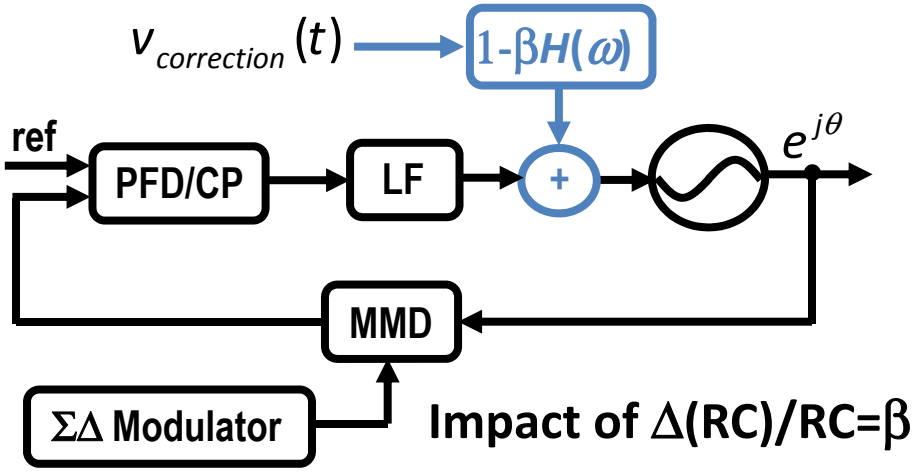
Applying Correction Signal Through MMD



Non-Ideal Impacts

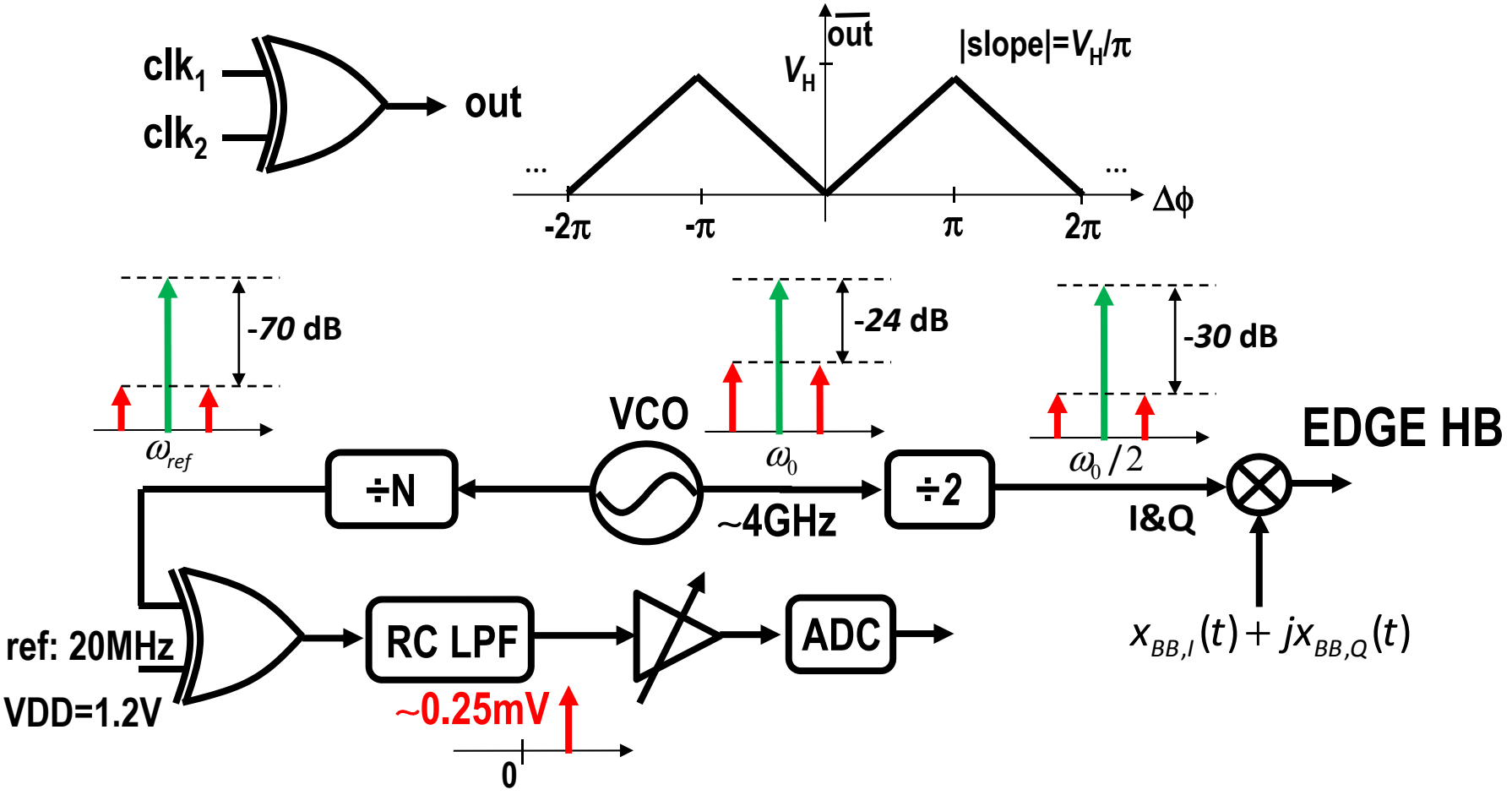
- The delay from PAD/PA to VCO included in '$\gamma e^{j\Psi}$' term
- For TX, PLL transfer function must be de-embedded
  - DC gain adjusted automatically: I_{CP} ,K_{VCO} not needed
  - But RC needs to be controlled
  - Simple RC-calibration sets time-constant accurately to < 1.5%





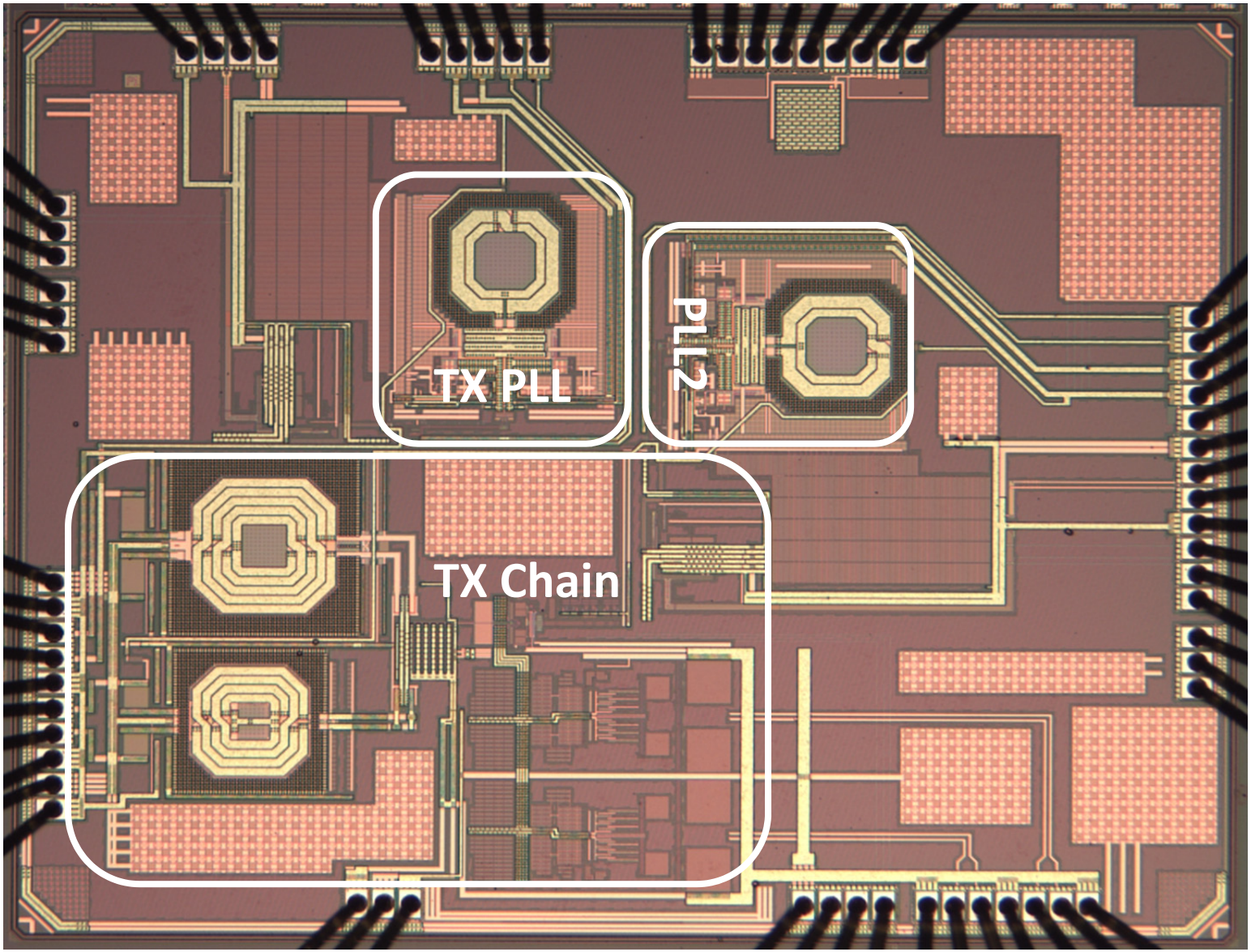
- RC inaccuracy has no impact in the case of multiple VCOs, as the correction signal is a tone

XOR, LPF, Pre-Amp & ADC Noise Requirements

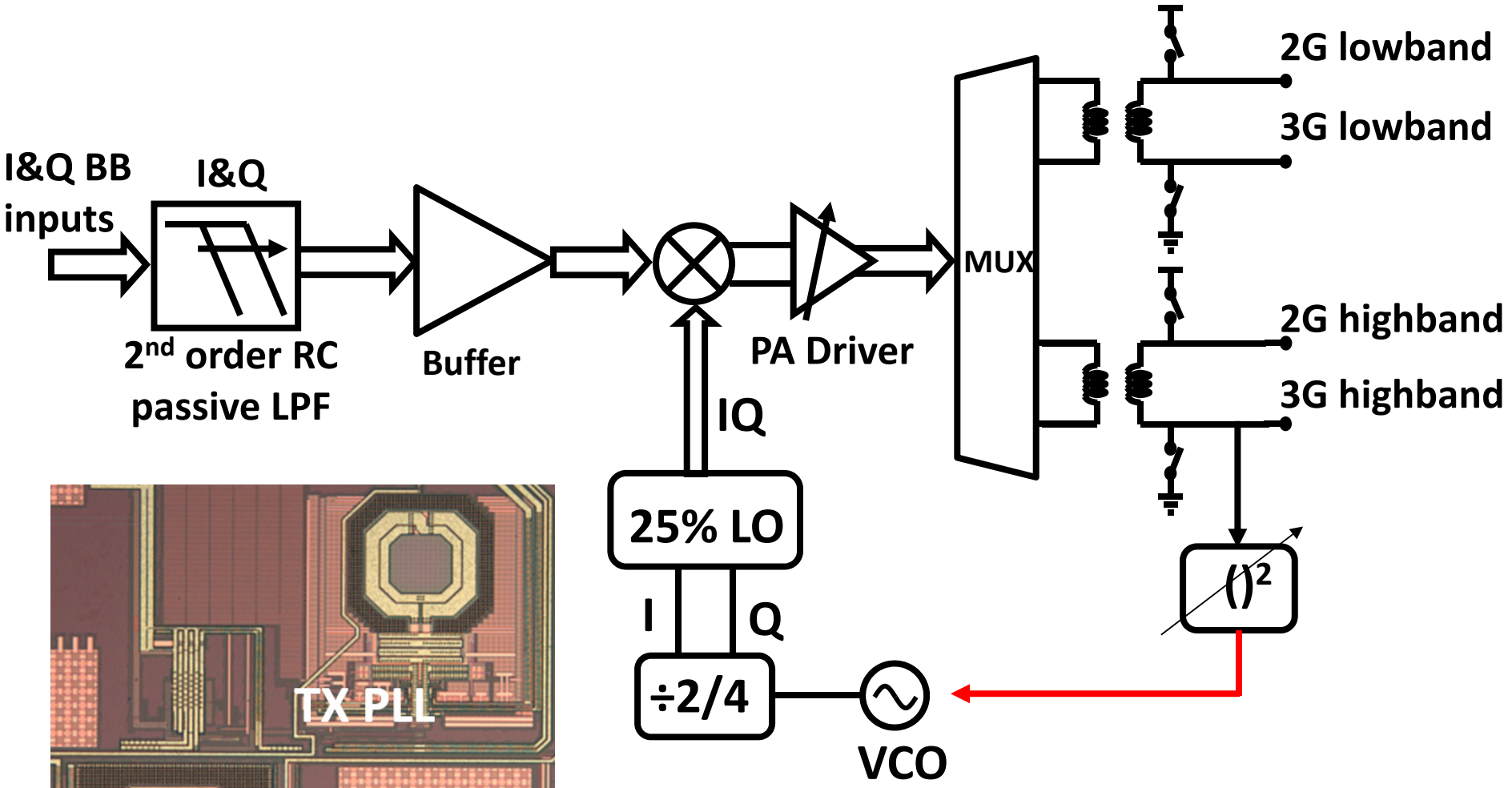


- Divider noise appears only at far-out frequencies; No impact
- Translated to dynamic-range of 74dB, w/ ADC full-scale of VDD
- A trivial pre-amplifier relaxes ADC requirements

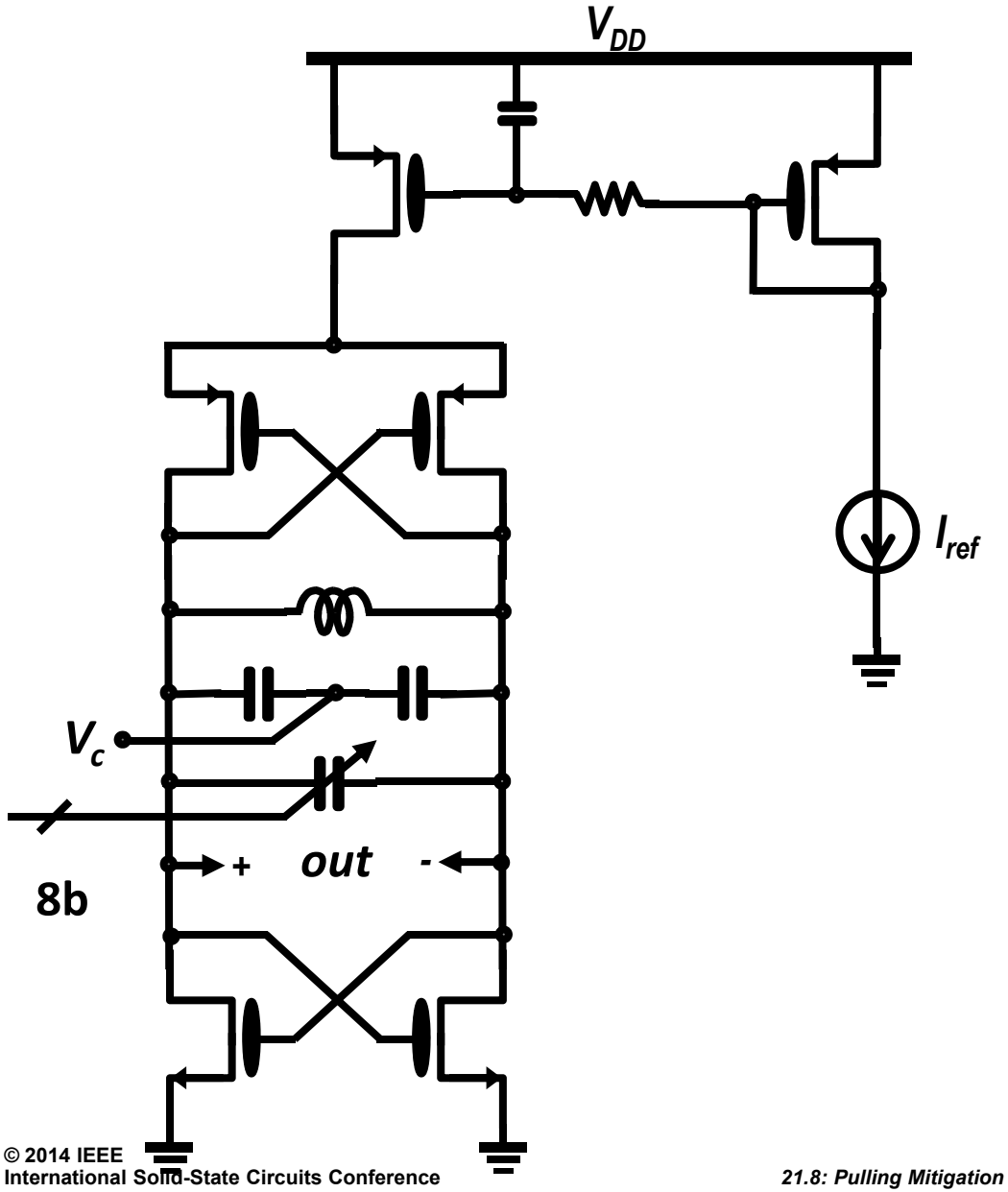
Die Photo

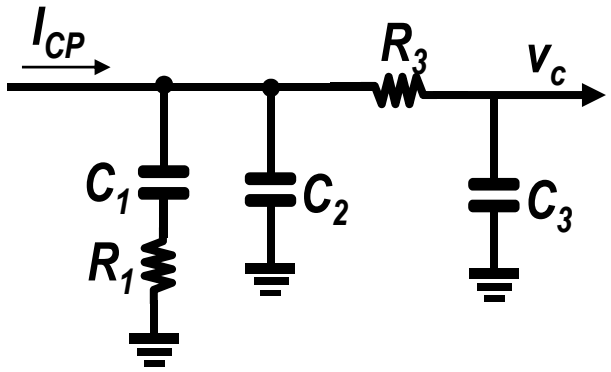


Transmitter Architecture



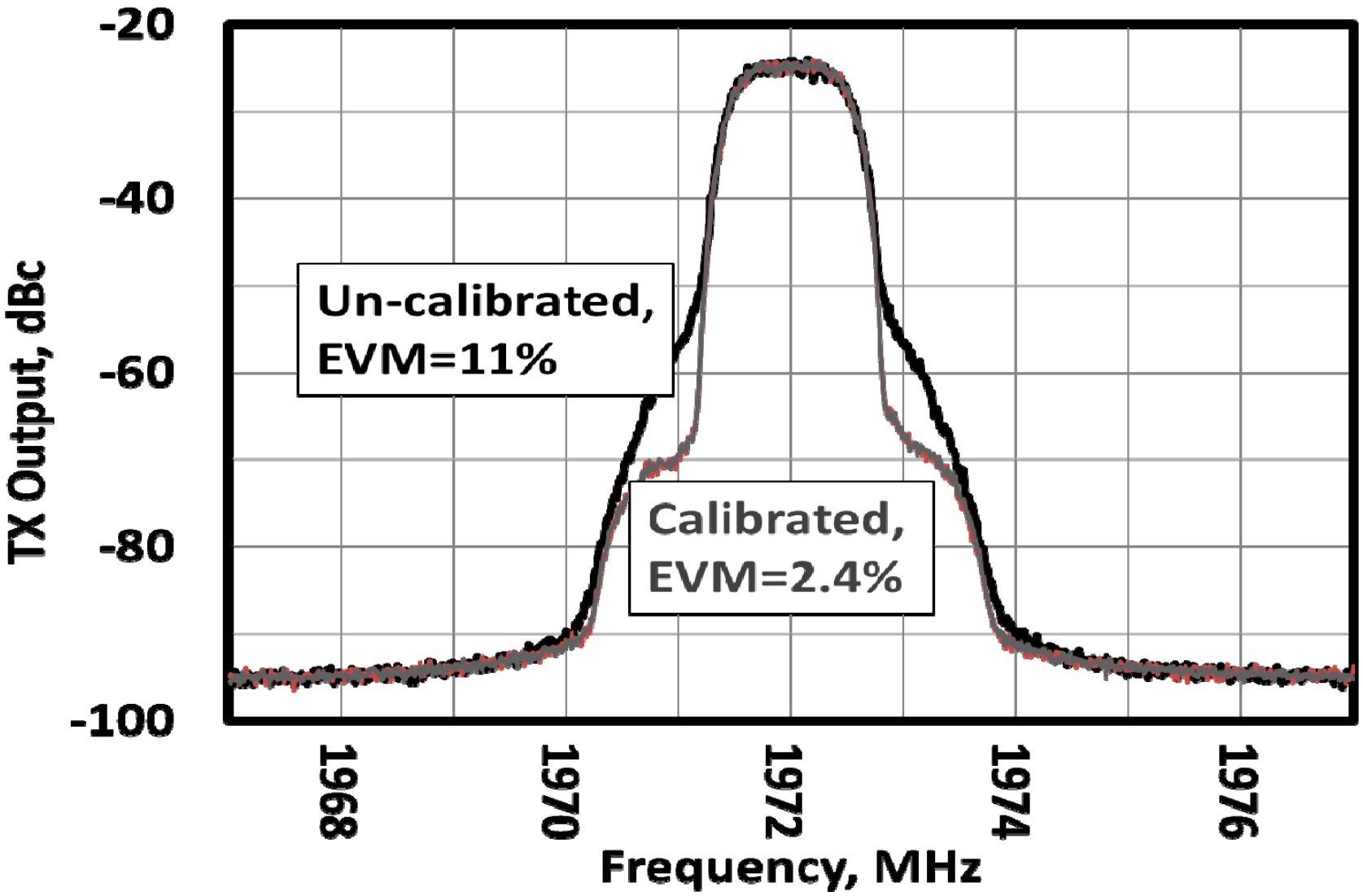
VCO and Loop Filter





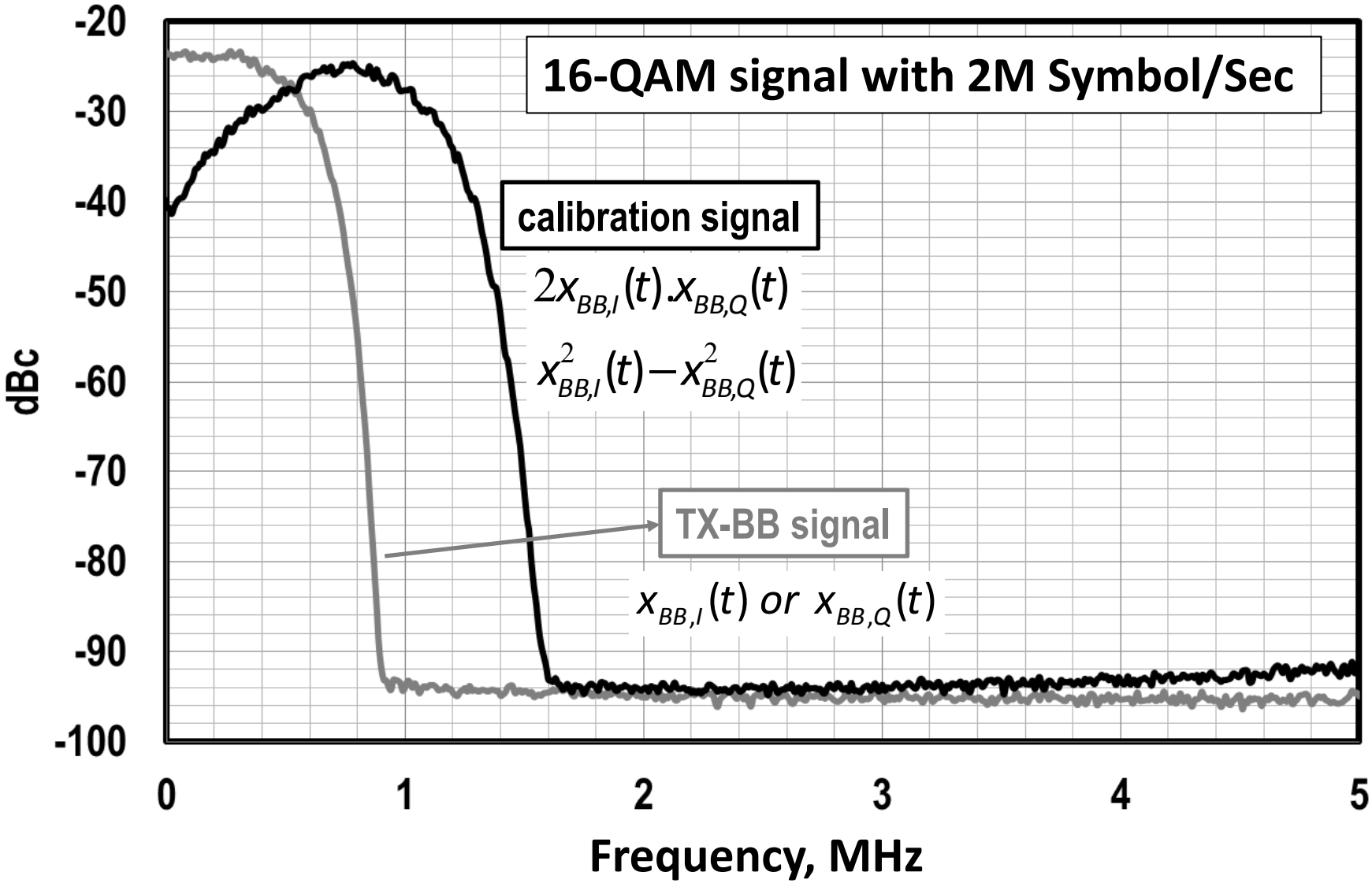
C_1=600pF
C_2=54pF
C_3=30pF
R_1=R_3=24KΩ

Modulation Spectrum Before and After Calibration

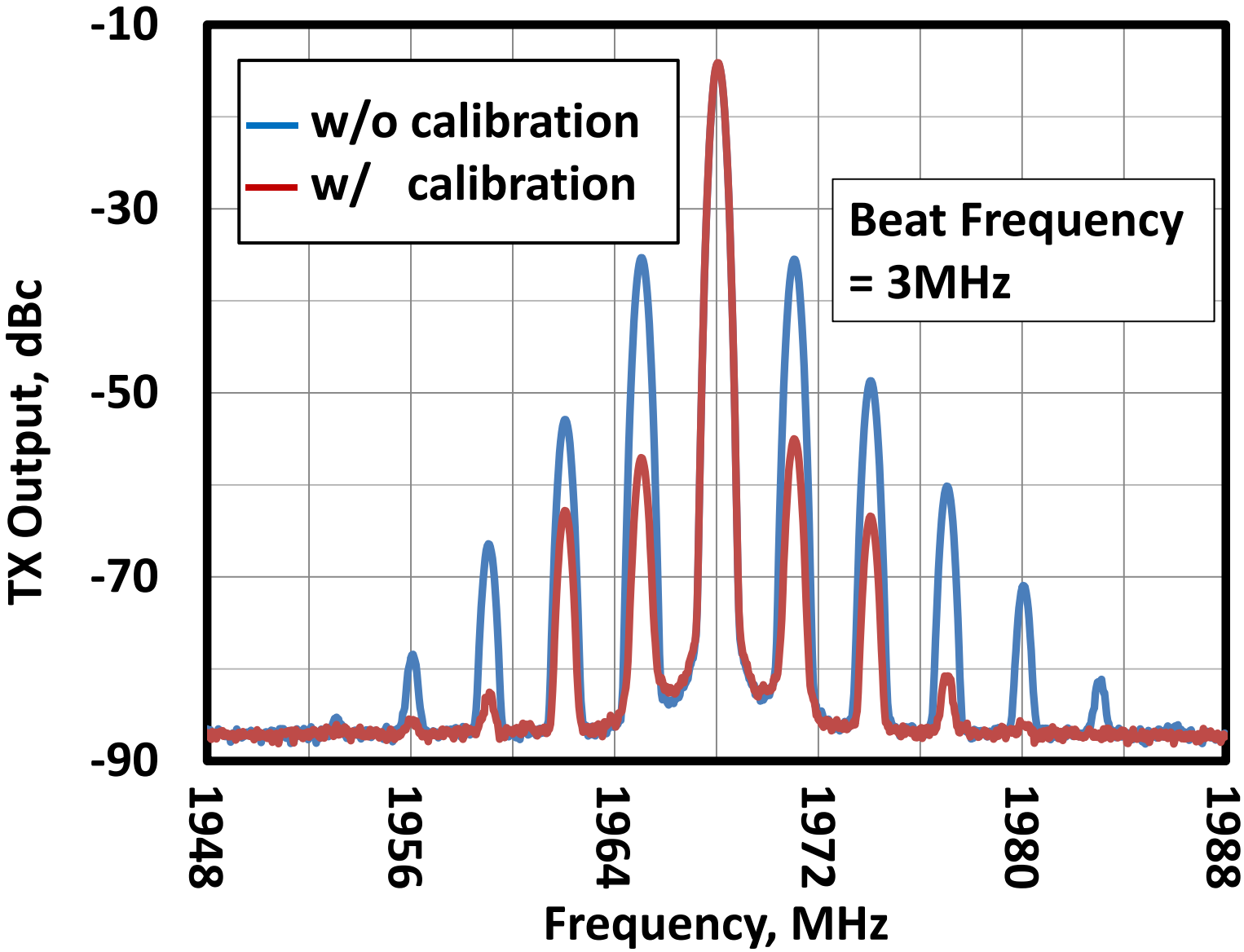


Out-of-band measured TX noise remains the same.

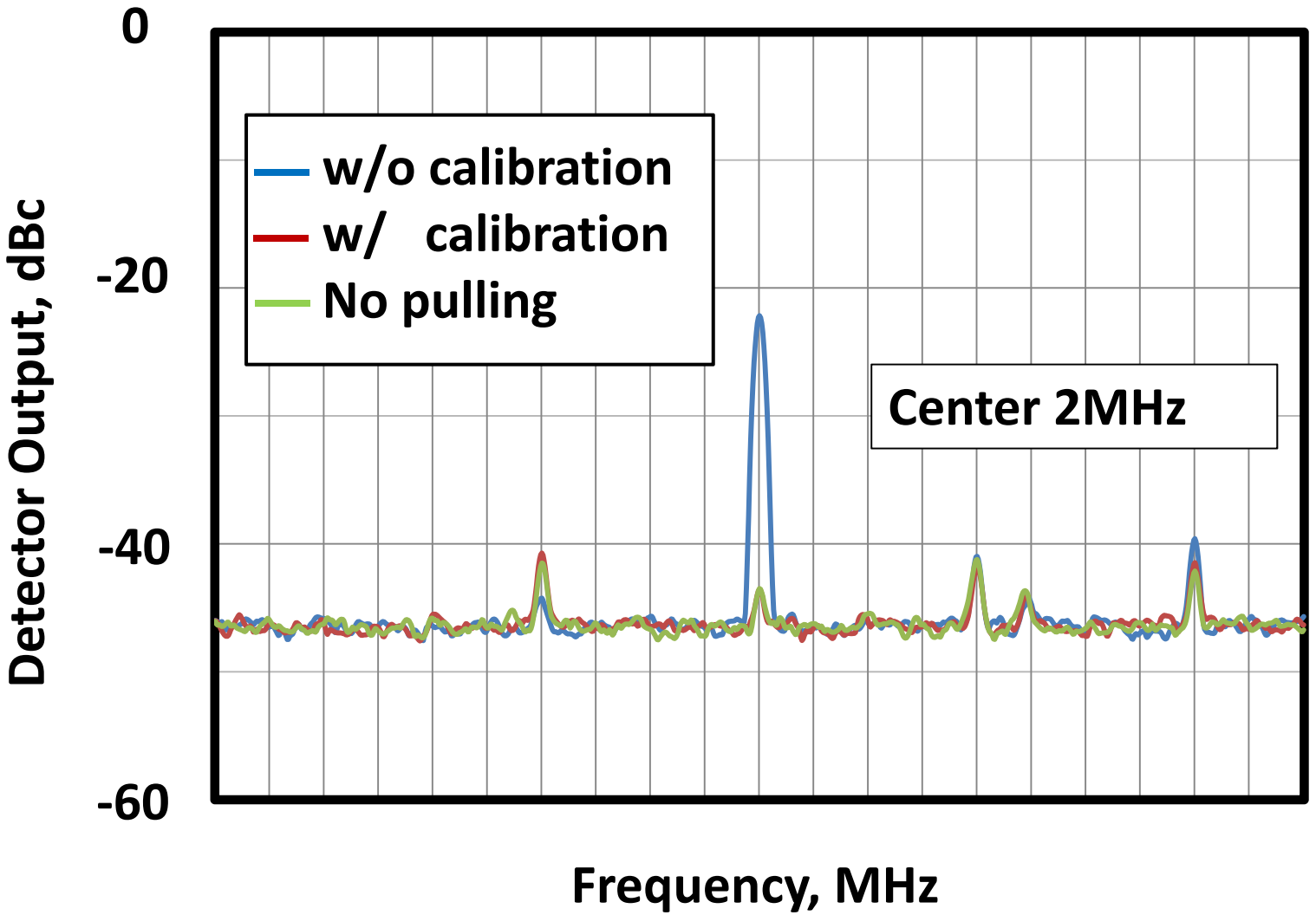
Input Baseband and Calibration Signal



Mutual Pulling Correction



Detector Output Before and After Calibration

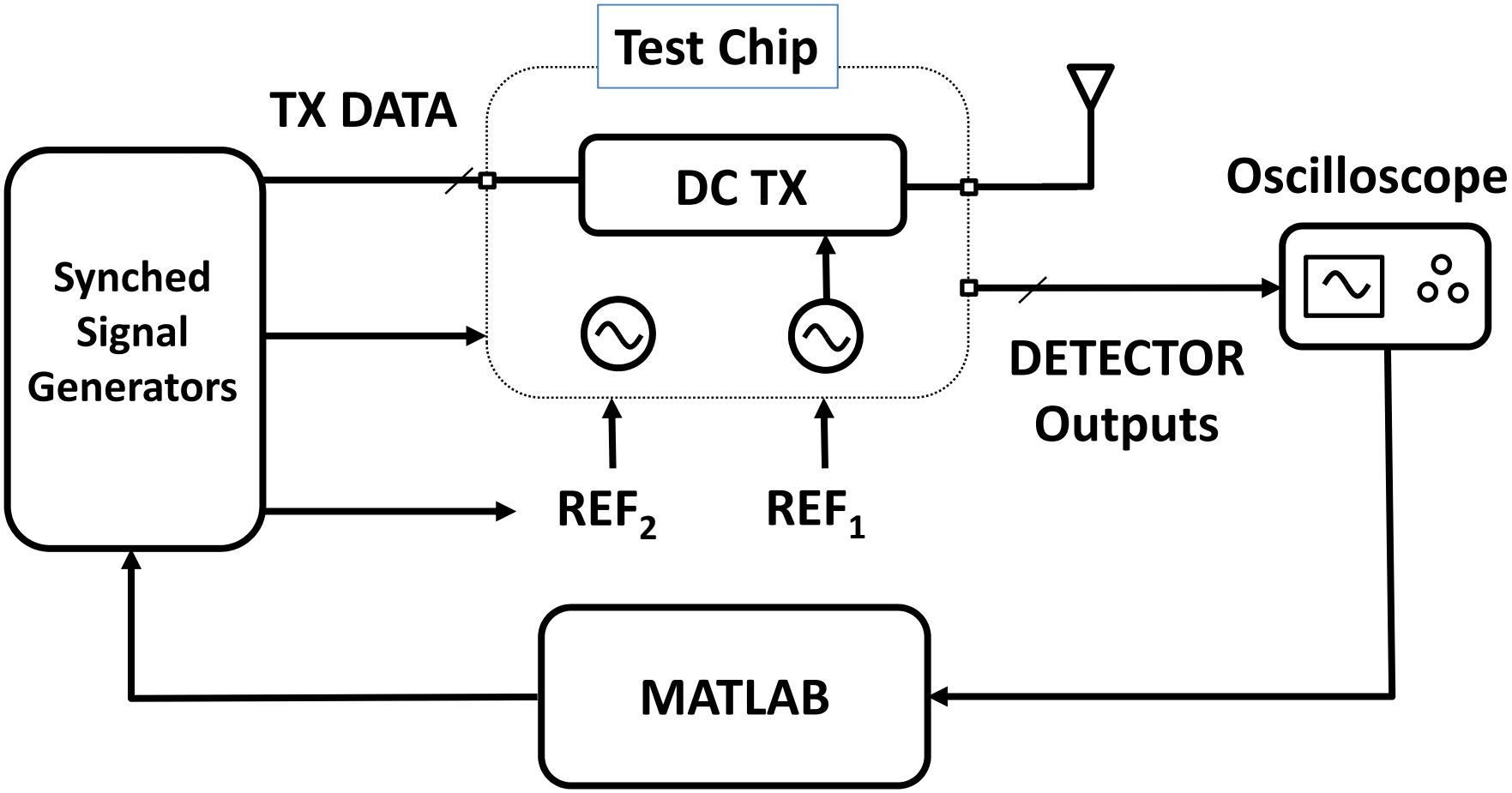


Baseband Inputs of TX: Quadrature signals at 1MHz

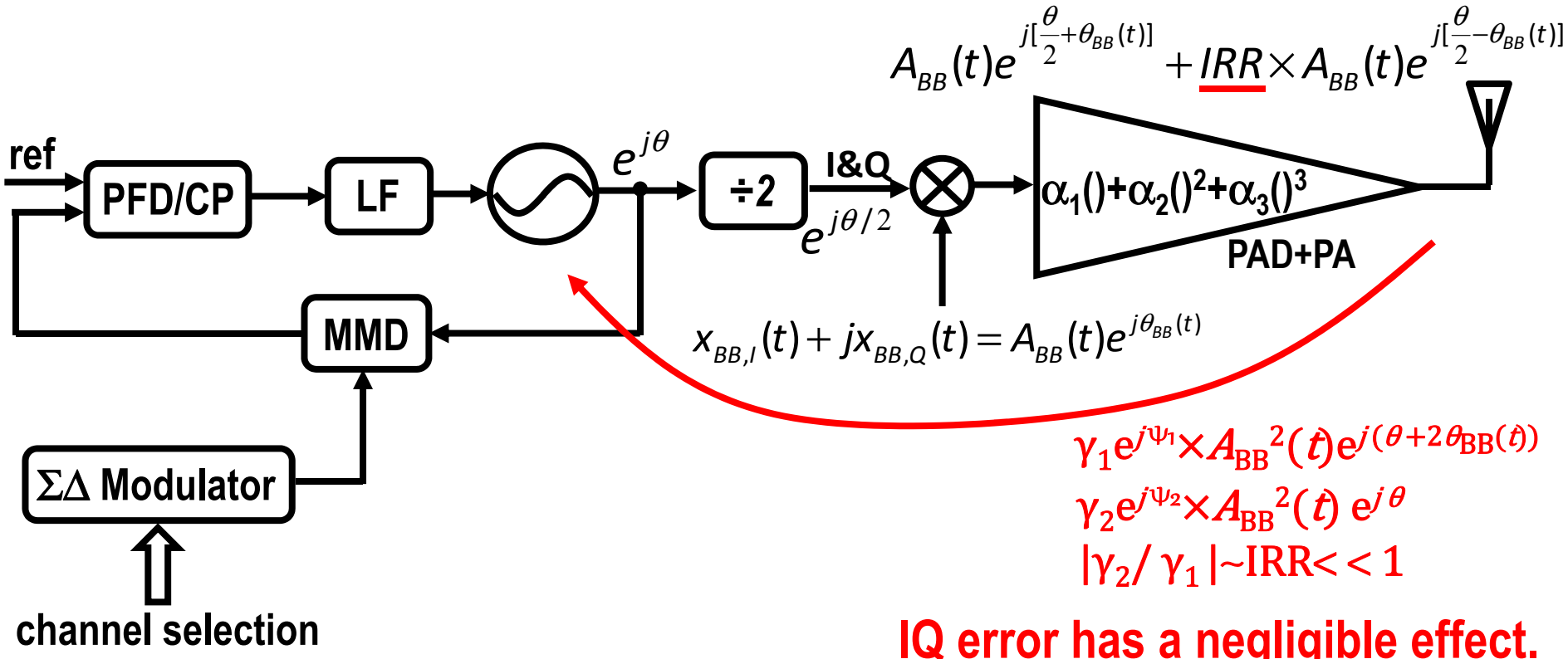
Conclusions

- Direct-conversion TX is low power & versatile but suffers from pulling
- Multiple close-by VCO's on chip due to FDD, CA, …
- A calibration technique to mitigate pulling presented
- Fully digital
- Negligible increase in power and area overhead
- Runs online without interrupting the TX or VCO's normal operations

Test Setup



Impact of IQ Mismatch



$\gamma_1 e^{j\Psi_1} \times A_{BB}^2(t) e^{j(\theta+2\theta_{BB}(t))}$

$\gamma_2 e^{j\Psi_2} \times A_{BB}^2(t)\, e^{j\theta}$

$|\gamma_2/\gamma_1| \sim IRR << 1$

IQ error has a negligible effect.

$$\frac{d\theta}{dt} = K_{VCO}\frac{I_{CP}}{2\pi}(\theta_{ref} - \frac{\theta}{N}) * h_{LF}(t) + \frac{\omega_0}{2QI_S}\{\gamma_1 A_{BB}^2(t)\sin(2\theta_{BB}(t)+\psi_1) + \gamma_2 A_{BB}^2(t)\sin\psi_2\}$$

final correction signal, independent of θ